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Low Temperature Electronics and Low Temperature Cofired Ceramic Based Electronic Devices

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PV 2003-27
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Miniaturization of electronic devices and improved system properties are the cornerstone for the development of advanced semiconductor electronic technologies for this century. Existing materials technologies and manufacturing processes reached a level-limiting stage. Therefore, further understanding of new materials and technologies and development of cost-effective manufacturing techniques is needed for a quantum jump in system properties and applications such as wireless telecommunication devices, military hardware, automotive electronics and the so-called emerging technologies. The latter include single electron transistors, nano-electronic devices, spintronics, and quantum computing.

The Electrochemical Society and The Electronics Division of The American Ceramic Society understand their responsibility and are the major facilitators for new materials development through information transfer by bringing together technical experts from diversified fields.

This volume contains 26 peer-reviewed papers and 3 extended abstracts from two symposia: "Low Temperature Electronics and Low-Temperature Co-fired Ceramic Based Electronic Devices", that were held during the Annual Meeting of The Electrochemical Society joint with The Electronics Division of The American Ceramic Society, October 12-16, 2003, in Orlando, Florida.

The symposia were international in flavor with attendees from Belgium, Brazil, Canada, France, Japan, Mexico, The Netherlands, and the USA. The main focus was on the use of cryogenic electronics for space applications and microelectronic devices for consumer applications. Beside the general trend to use Custom-off-the-Shelf (COTS) components, there exists a strong interest in using SiGe and even Ge-based devices. There is a large interest in low temperature studies, not only because of the fundamental physics involved, but also because of the improved device performance. Nowadays, there is research carried out on both deep submicron CMOS devices. Important issues, however, remain the control of self-heating effects and the packaging aspects. Also focus was on new and futuristic LTCC materials based high-density packaging, including areas such as material and circuit design, manufacturability, reliability and cost-effectiveness, and thermoelectric materials.
The editors would like to thank the following symposia co-organizers: Dr. T. R. Armstrong, Oak Ridge National Laboratory; Professor A. S. Bhalla, The Pennsylvania State University; Professor M. J. Deen, McMaster University, Hamilton, Ontario; Professor G. S. Nolas, University of South Florida, Dr. R. E. Sah, Fraunhofer Institute, Freiburg, Germany; and Professor Oleszek, University of Colorado.

We acknowledge both the invited and contributed authors for making these symposia possible by sharing their perspectives and insights and putting considerable effort into the preparation of the camera-ready manuscript; the contribution of the Session Chairs in chairing and guiding the sessions; paper reviewers; and the Officials of both Societies for making this endeavor a successful one.

January 2004

Cor Claeys
Winnie Wong-Ng
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LOW TEMPERATURE ELECTRONICS
HALO EFFECTS ON 0.13 \,\mu m FLOATING-BODY PARTIALLY DEPLETED SOI n-MOSFETS IN LOW TEMPERATURE OPERATION

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ABSTRACT

This work studies the effect of halo implantation on the electrical characteristics of deep-submicrometer partially depleted SOI nMOSFETs during low temperature and floating body operation. Parameters such as the Drain Induced Barrier Lowering and the device thermal resistance have been investigated. It is shown that the combination of floating body operation with halo implantation degrades the DIBL in the temperature range studied (90 – 300 K) in comparison to devices that did not received this implantation. The halo region causes a more pronounced negative output conductance than for the transistors without a halo implantation. An estimation of the temperature rise for a given dissipated power in both types of devices is made, based on the thermal resistance, which is derived from the output characteristics in function of the temperature.

INTRODUCTION

Nowadays, the Silicon-On-Insulator (SOI) MOS technology is considered as an excellent option to address the scaling problems in the bulk counterpart for low-power, high-performance applications. The reduced junction capacitance and absence of latch-up in SOI allow circuits to operate at higher speed or with reduced power for the same speed than for bulk CMOS (1). However, the device downscaling in the deep-submicrometer regime necessitates channel engineering by the use of halo (or pocket) implantations to avoid the leakage current and short-channel effects that may degrade the device output characteristics (2-3).

Partially depleted SOI MOSFETs with floating-body (FB) present better speed and power consumption performance compared to their bulk counterparts (1) thanks to the occurrence of FB effects, which increase the potential of the device body region. The
problems associated with the FB are the kink effect, that degrades the output conductance (go) in saturation, and the reduced drain breakdown voltage.

Improved device characteristics are obtained at low temperatures, due to the increased carrier mobility and velocity saturation, reduced inverse subthreshold slope and junction capacitances, finally resulting in better switching characteristics than at room temperature without scaling the device dimensions (4).

In this work the influence of the combination of low temperature operation and an halo implantation step on the electrical characteristics of 0.13 μm long partially depleted SOI nMOSFETs with floating body will be analyzed. The Drain Induced Barrier Lowering (DIBL) and the self-heating (SH) effect will be pointed out. Experimental results, two-dimensional simulations and modeling are used to support the analysis.

**PROCESS DESCRIPTION**

The studied nMOS devices were fabricated using the IMEC's 0.13 μm SOI CMOS technology. Standard UNIBOND wafers with a film thickness of 200 nm and 400 nm thick buried oxide were used. The initial silicon film thickness is reduced to about 100 nm by oxidation and etching. For active region isolation the standard PELOX technique has been implemented. The gate stack consists of a 2.5 nm thick nitrided oxide (NO) and a 150 nm thick polysilicon layer. DUV 193 nm optical lithography is used for gate patterning. Shallow source and drain extensions are formed by low energy ion implantation of arsenic, followed by the halo angled implants (3 x 10^{13} cm^{-2} BF_2 at 65 keV) to control the short-channel characteristics. Devices without the halo implantation have also been fabricated following the same process sequence presented above, except for the halo implant step.

The samples were cooled down to 90 K and after temperature stabilization the measurements were performed using a HP4156C semiconductor parameter analyzer. All the devices have been measured starting from the lowest temperature (90 K) up to room temperature (300 K). An L-array containing 0.08, 0.1, 0.11, 0.12, 0.13, 0.14, 0.15, 0.18, 0.2, 0.22, 0.25, 0.3, 0.4, 0.5, 0.6, 0.8, 1.0, 5.0, 10.0 μm long devices with a constant channel width (W) of 10 μm has been used for the measurements.

**DIBL EVALUATION**

The DIBL effect constitutes an important feature to be addressed in deep-submicrometer transistors (5-6). As reported in the literature, the DIBL does not degrade as the temperature is lowered (5). In order to define the DIBL we used the expression [1]:

\[
\text{DIBL} = \frac{V_T(V_{DS} = 0.1V) - V_T(V_{DS} = 1.5V)}{1.5 - 0.1} \tag{1}
\]
where $V_t(V_{DS}=0.1\ V)$ and $V_t(V_{DS}=1.5\ V)$ are the threshold voltages extracted with an applied drain bias ($V_{DS}$) of 0.1 V and 1.5 V, respectively. The threshold voltage extraction has been performed using the double derivative technique (7).

Prior to the DIBL evaluation, figure 1 presents the extracted threshold voltage ($V_T$) as a function of mask channel length ($L_{mask}$) for the nMOS devices at room temperature and at 90 K.

![Figure 1. Threshold voltage as a function of the mask channel length ($V_{DS}=0.1\ V$) for nMOS transistors at 300 K and 90 K (8).](image)

From figure 1 one can see the occurrence of the conventional reverse short-channel effect on the threshold voltage for halo devices, i.e., an increase of $V_T$ for a lower mask channel length, due to the interaction between the halo charges with those implanted for $V_T$ adjust. On the other hand, the no halo transistors show a clear degradation of $V_T$ with the channel length reduction, due to short-channel effects. This points out that the HALO dose efficiently minimized such phenomena. For mask channel lengths below 0.2 $\mu$m an appreciable threshold voltage reduction is observed in the nMOS transistors without halo at room temperature. By decreasing the temperature down to 90 K the minimum channel length for a similar threshold voltage degradation decreases to about 0.15 $\mu$m.

The maximum transconductance has been extracted for all studied devices with and without halo at 300 K and 90 K and the results are compared in figure 2.

Generally, the maximum transconductance of the no halo devices is higher at any channel length and for both temperatures. This is due to the lowering of the mobility by Coulombic scattering at the ionized channel dopants, which should be more pronounced at cryogenic temperatures. At the same time, there is a reduction in the ratio between the maximum $g_m$ at 90 K and 300 K for the 0.13 $\mu$m device in comparison to the 10 $\mu$m transistor, pointing to the role of the halo doping in lowering the mobility.
The basic conclusion derived from figures 1 and 2 is that the body region of 0.13 μm transistors with halo presents high doping level than those without this implantation.

Figure 3 shows the measured DIBL at 300 K and at 90 K as a function of the mask channel length.

As the channel length reduces the DIBL becomes more pronounced. Comparing the results for transistors with and without halo, for reduced channel lengths the DIBL is larger in halo transistors than in no halo ones. The difference increases as the channel length is smaller which reflects the increase of the doping level as the channel length shrinks.
Concentrating the DIBL evaluation on the 0.13 μm transistors as a function of the temperature, the results of figure 4 have been obtained.

![Figure 4 - Extracted DIBL as a function of the temperature for halo and no halo doped 0.13 μm long transistors.](image)

The DIBL is almost independent on the temperature in both studied cases, which is in agreement to the results reported in ref (6).

In order to gain physical insight in the obtained results, two-dimensional simulations were performed for room temperature operation (10). Models accounting for mobility degradation depending on concentration and carrier-to-carrier scattering, Auger recombination, bandgap narrowing, impact ionization and energy balance equations were included in the simulation files. Default simulator coefficients for all parameters have been employed with no optimization, which is beyond the scope of this physical analysis and may affect the quantitative results but does not affect the qualitative analysis and trends.

The simulations were focused on 0.13 μm transistors. Instead of the nitrided oxide insulator of the fabricated devices we used 2.5 silicon dioxide without the tunneling model. A uniform boron doping level of 8 x 10^{17} cm^{-3} and 5 x 10^{17} cm^{-3} has been used for halo and non halo devices, respectively. The remaining parameters such as source/drain extensions depth and doping have been kept identical in both structures. A 7 nm per decade decay in n-doping density has been used in all junctions. Figure 5 gives the simulated drain current (I_{DS}) as a function of gate voltage (V_{GP}), with V_{DS} = 0.1 V and 1.5 V, for devices with and without halo.
Figure 5 – Simulated $I_{DS}$ versus $V_{GF}$ curves for halo and no halo 0.13 $\mu$m transistors.

By using the simulated results of figure 5 and equation [1] the DIBL results of both structures have been extracted and compared to the experimental results from figure 4 as indicated in table 1.

Table 1 – Comparison between the extracted DIBL for halo and no halo transistors.

<table>
<thead>
<tr>
<th>DIBL (x10^-3)</th>
<th>Halo</th>
<th>no halo</th>
<th>ADIBL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation</td>
<td>118</td>
<td>79</td>
<td>39</td>
</tr>
<tr>
<td>Experimental</td>
<td>142</td>
<td>100</td>
<td>42</td>
</tr>
</tbody>
</table>

The simulated results for DIBL are smaller than those experimentally measured, which can be justified by the differences in the doping level for the simulated structures. Notwithstanding these differences, the obtained trends are in full agreement to the experimentally extracted ones and allow the study of the physical reasons for the degraded DIBL in halo transistors.

In order to verify the impact of the floating body, an additional contact has been added to the channel region and tied to ground (GND). This additional contact has the same function as the body contact usually implemented in partially depleted SOI MOSFETs. The simulated results in this situation are shown in figure 6.
As can be seen from figure 6, a negligible DIBL is found in both type of devices. In addition, and as expected, the DIBL becomes larger in a no halo device than in the halo one, as the halo region is efficiently blocking the drain potential penetration to the channel. To fully cover the possible reasons for the obtained results, the remaining variable to be addressed is the impact ionization effect on DIBL. The impact ionization model has been removed from the simulation files and the body was made floating again. Figure 7 summarises the set of simulated situations with $V_{DS}$ of 1.5 V for the non halo transistor only.

One can see from figure 7 that the simulated results with the impact ionization (I. I.) model and body tied to GND and without I. I. but with floating body are practically the same. Similar results have been obtained for halo devices. Therefore, it can be concluded that the combination of floating body and impact ionization is responsible for the above reported higher DIBL obtained in both device types. The higher doping level in halo devices increase the potential barrier for the holes generated by the I. I. mechanism in the drain side region. These holes increase the body potential causing the observed DIBL effect. When the body region is tied to ground, the majority of the hole current is collected in this contact and does not reach the source junction.
SELF-HEATING EFFECT

It is well known that SOI nMOSFETs suffer from the self-heating effect as a consequence of the low thermal conductivity of the buried oxide (which is about two orders of magnitude smaller than that of the silicon substrate). The self-heating effect is characterized by the presence of a negative output conductance region in the drain current (\(I_{DS}\)) versus drain voltage (\(V_{DS}\)) curve. The temperature rise also increases the impact ionization current in SOI MOSFETs by locally providing a source for carrier heating, thereby reducing the mobility (11-12).

A comparison between the measured drain output conductance (\(g_{D}\)) at 90 K is plotted in figure 8 as a function of \(V_{DS}\) for different \(V_{GT}\), where \(V_{GT}\) is the gate voltage overdrive (\(V_{GT}=V_{GR}-V_{T}\)). In these curves the solid symbols refer to the halo doped device and the open symbols to the no halo transistor.

The presence of a negative \(g_{D}\) indicates the occurrence of self-heating in the halo transistors, even for reduced \(V_{GT}\). However, this effect has not been observed for the no halo devices. There is an indication that, in addition to the contribution of the buried oxide thermal resistance, as the silicon film becomes higher doped the thermal response of the structure is modified.
In order to verify the thermal resistance associated to each studied structure the $V_{GT}$ has been increased to 1.8 V to induce the SH effect in both devices, as for example indicated in figure 9 at 95 K, and $I_D$ versus $V_D$ curves were extracted. To perform the set of measurements the temperature has been varied in the sequence 95 K, 125 K, 150 K, 175 K, 200 K, 225 K, 250 K and 300 K.

![Figure 9 - Drain output conductance as a function of the drain voltage at 95 K ($V_{GT}$=1.8 V) for devices with and without halo.](image-url)
Following the approach of Jomaah et al. (14–15), the thermal resistance ($R_{th}$) can be extracted from experimental data using the equation:

$$R_{th} = \frac{g_{DS}}{\frac{dI_{DS}}{dT}}$$  \hspace{1cm} \text{(2)}$$

where $g_{DS}$ is the drain output conductance in saturation, $I_{DSsat}$ is the corresponding drain current and $dI_{DS}/dT$ the temperature sensitivity of the self-heated device. The $dI_{DS}/dT$ term is obtained by taking the difference between two $I_{DS} \times V_{DS}$ curves in different temperatures from the measured set.

Figures 10 (A) and (B) give the $(dI_{DS}/dT)^{-1}$ curves as a function of $V_{DS}$ extracted in the indicated temperature range for transistors without and with halo, respectively, with a $V_{GT}$ of 1.8 V.

![Figure 10](image)

For an operation temperature of 95 K one can observe that the no halo transistor presents an increase of $(dI_{DS}/dT)^{-1}$ for $V_{DS}$ larger than 1.75 V. This effect is associated with the parasitic bipolar action at higher $V_{DS}$, increasing the drain current. In order to avoid the influence of this effect on the results, only the region up to a $V_{DS}$ of 1.75 V will be considered in the remaining part of the work.

Combining the results given in figure 10 and equation [2] the thermal resistance of the transistors ($R_{th}$) is calculated as a function of the temperature ($V_{GT}$ of 1.8 V) in the range of 95 K to 200 K, as shown in figure 11. In both cases $R_{th}$ has been calculated at the point $V_{DS} - V_{DSsat}$ equal to 0.75 V, where $V_{DSsat}$ is the drain saturation voltage which has been extracted according to the procedure described in (17). The figure also shows for a few temperatures the values of the thermal resistance extracted for halo devices with channel lengths ($L$) of 0.18 $\mu$m and 0.4 $\mu$m (different symbols in figure 11), in order to
verify if the \( L \) value can influence the extracted results. The temperature range is limited to 200 K as for higher temperatures the self-heating becomes less pronounced which may lead to a too low extracted thermal resistance values due to a loss of accuracy in the calculation method.

![Graph](image)

Figure 11 – Calculated thermal resistance in the range 95 K to 200 K for halo and no halo devices (16).

There is an agreement between the calculated \( R_{TH} \) in all halo transistors, mainly for the devices with a \( L \) of 0.13 \( \mu \)m and 0.18 \( \mu \)m at 95 K, where the thermal resistance is more pronounced. As shown in figure 1, for channel lengths smaller than 0.3 \( \mu \)m the fabricated devices start suffering from reverse short-channel effects, indicating a higher doping profile.

On the other hand, the \( R_{TH} \) for the no halo device is smaller than in the halo ones for all studied temperatures. Although the difference in the resistance is in the order of 15 % at lower temperatures, there is an indication that the halo region can induce a larger thermal resistance.

Considering that the temperature rise in the device is directly proportional to the dissipated power, it is then possible to estimate the device temperature rise (\( \Delta T \)) as a function of \( V_{DS} \) using the calculated \( R_{TH} \), by means of equation [3](14):

\[
\Delta T = R_{TH} \cdot I_{DS} \cdot V_{DS}
\]  

The calculated \( \Delta T \) for halo and no halo devices at a temperatures of 95 K, 125 K and 175 K in function of \( V_{DS} \) are plotted in figure 12. The results are limited to the range of \( V_{DS} \) values where the parasitic bipolar action is negligible in both cases.

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Figure 12 – Estimated temperature rise as a function of $V_{DS} - V_{DSat}$ for halo and non-halo $0.13 \mu m$ MOSFETs operating at 95 K, 125 K and 175 K (16).

For an ambient temperature of 95 K, the maximum device temperature rise changes from about 90 K (no halo) to 135 K (halo) when the drain voltage is increased due to a more pronounced self-heating effect in halo transistors. The temperature increase due to self-heating is reduced for higher operating temperatures.

CONCLUSION

This paper studied the trade-offs imposed by the halo implantation step on the electrical characteristics of floating body partially depleted SOI nMOSFETs in deep-submicrometer regime and low temperature operation. DIBL and self-heating effect have been critically discussed.

It has been shown that the halo implantation combined with the floating body operation results in an increased impact ionization current. This impact ionization current is responsible for the higher DIBL observed in comparison to devices without the halo implantation.

The self-heating effect is more pronounced in halo transistors than in no halo ones. The halo implanted transistor presents larger thermal resistance than the no-halo one in all studied temperatures. Due to this large thermal resistance, a more pronounced temperature rise is found in the halo devices when the drain voltage is increased.
ACKNOWLEDGMENTS

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REFERENCES

EMERGING DOUBLE-GATE MOS DEVICES TECHNOLOGY

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Abstract. We are facing to the red brick wall for further MOSFET scaling-down. By shrinking the device size, the severe degradation of the device performance such as the short-channel effects (SCEs) appears in a conventional bulk MOSFET. To overcome the difficulties, double-gate (DG) MOSFETs or X-MOSFETs are recognized as the most promising candidate for future ULSI circuits. The R&D of the DG MOS devices are reviewed, and two types of DG MOSFETs fabricated by using newly developed processes, i.e., a Fin-type DG MOSFET (FXMOSFET) and a vertical-type DG MOSFET (IMOSFET) are presented. These emerging DG MOS devices will become available soon.

INTRODUCTION

The ITRS semiconductor roadmap (1) followed by the Moor's law indicates that we are facing to the red brick wall as shown in Fig.1. The aggressive scaling-down of a conventional MOSFET causes the increase in a leakage current through the gate insulator and between the source and drain, and the degradation of the device performance, namely, the short-channel effects (SCEs). To suppress the tunneling leakage current through the SiO2 gate insulator, alternative gate dielectrics with high-K have recently been investigated (2). From the viewpoint of the MOSFET device structure, on the contrary, the most severe issue caused by shrinking the device size is the SCEs. The SCEs are due to the interference between the drain and source. The MOSFET is a three terminal device, and the drain current output should be controlled only by the gate signal input. Therefore, this interference means the weakening of the gate control. In other words, we need more negative gate bias to turn off the channel in the n-channel case. This threshold voltage (Vth) shift in the negative direction (for n-channel) is called as Vth roll-off, and is a very tough issue in the integrated circuit operation. Simultaneously, the degradation of the subthreshold characteristic, i.e., the increase in a subthreshold slope (S-slope) and the consequent increase of the off-state current occur. To interrupt the interference between the drain and source caused by the
Difficulties
- Increase in leakage current
  Between source and drain
  Through gate insulator (SiO₂)
- Short channel effects
- Threshold voltage roll-off
- Degradation of S-slope

Fig.1  ITRS roadmap for semiconductor and difficulties caused by the device scaling-down. We are facing to the red brick wall.

Fig.2  Evolution of the MOSFET structure: (a) a conventional single-gate MOSFET, (b) an ultra-thin SOI MOSFET (pseudo-XMOSFET), (c) a double-gate MOSFET (XMOSFET)
shrinkage of a conventional shingle-gate MOSFET shown in Fig. 2(a), a fully depleted (FD) ultra-thin SOI MOSFET (Fig. 2(b)) has been investigated. The path from the drain to source through the substrate is cut off in this structure, which is effective to suppress the short channel effects (3, 4). However, the shielding of the drain influence is not perfect even in the FD SOI MOSFET. Because the drain electric field could affect the source through the buried oxide layer in a short-channel SOI MOSFET. To overcome the drain-source interference completely, the double-gate (DG) MOS or XMOS structure (Fig. 2(c)) is most desirable (5).

In the paper, we review the R&D of the DG MOS devices, and the two types of DG MOSFETs fabricated by using newly developed processes, i.e., a Fin-type DG MOSFET (FXMOSFET) and a vertical-type DG MOSFET (IMOSFET) are presented as an emerging DG MOS devices technology.

DOUBLE-GATE (DG) MOSFET CONCEPT

The DG MOS device was originally proposed in the early 80's from Electrotechnical Laboratory (ETL) (5). The DG MOS device has two gates sandwiching the thin Si channel and was originally named XMOS from the resemblance of the Greek letter xi (Ξ) corresponding to the English letter X. This DG structure was thought out to prevent the performance degradation caused by MOS scaling-down, where the two gates shield the channel from the electrical interference between the drain and source. Two gates and a thin channel can cut off the roundabout path between the source and drain, and even the influence of the drain electric field to the source. These basic characteristics were shown in the simulation (5, 6) and certified by the experimental device (7).

![Fig. 3](image)

(a) Planar-type  (b) Fin-type  (c) Vertical-type

Fig. 3 Three types of the double-gate (DG) MOSFET structure: (a) a planar-type, (b) a Fin-type, (c) a vertical-type. The issue is how to fabricate.
There are three types of the DG MOSFET structures, i.e., a planar-type, Fin-type, and vertical-type, as shown in Fig. 3. The issue is how to fabricate the self-aligned double-gate with Si technology compatibility. The planar-type DG MOSFET has the most similar device configuration to the conventional bulk single-gate MOSFET. Therefore, the planar-type DG MOSFET enjoys the easiness of the circuit design. However, the fabrication of the original planar-type XMOS has been very difficult, and the pioneering experimental planar-type XMOS (8, 9) were not truly self-aligned DG XMOS, although the sophisticated planar-type DG MOSFETs have been reported recently (10, 11). On the contrary, the vertical-type and Fin-type XMOSFET enjoy relatively simple processes to fabricate the self-aligned double-gate. In these three-dimensional DG MOSFETs, the two gates are automatically self-aligned, because the gate areas are formed after the fabrication of the fin or the vertical channel wall. The gate-all-around-type MOSFET reported by IMEC (12) and Toshiba (13) is also categorized as a double-gate MOS device. However, the Fin-type firstly reported from Hitachi in 1989 (14) has investigated widely. In the fin-type DG MOSFET has its source, drain, and one of the gates on the same plane. The DG MOSFETs have many advantages: 1. high SCEs immunity, 2. low S-slope, 3. double drive current, 4. low gate induced drain leakage (GIDL). These superior advantages result from the complete shielding of the drain influence. Also, the DG MOSFET does not need the channel impurity control for scaling-down. This is the additional advantage of the DG MOSFET. In the aggressively scaled MOSFET the fluctuation of the impurity in the channel causes the fluctuation of $V_a$. Instead, the gate engineering is needed in the DG MOSFET, which is the important issue for the integration of DG MOSFETs.

EMERGING DG MOSFETS

New Fin-type DG MOSFET (FXMOSFET)

The Si-fins have usually been fabricated by using the conventional reactive ion etching (RIE), i.e., the physical plasma etching (15-20). However, the cross-sections inevitably become trapezoidal or a bell-shape. The distributed fin width results in the variation of $V_a$. The fabrication of the ultra-thin fins necessary for the SCEs suppression is also difficult by RIE. In addition, the RIE process may cause radiation damages. To solve the fin-fabrication issues mentioned above, the fabrication method of the rectangular fins using an orientation-dependent wet etching and a (110) SOI wafer has been proposed (21, 22).

Figure 4 indicates the main fabrication process flow of the Fin-type DG MOSFET (FXMOSFET). A starting material to fabricate an ideal rectangular Si-Fin is a p-type
Further narrowing with DHF.

Fig. 4 Main fabrication process flow of the Fin-type DG MOSFET (FXMOSFET) by using a (110)-oriented SOI wafer and an orientation-dependent wet etching.

(110)-oriented SOI wafer. The initial thicknesses of the (110) SOI and buried oxide (BOX) layers are 100 nm and 300 nm, respectively. First, the heavily doped areas for the source-drain contact regions are formed. The resist pattern to designate the fin pattern is formed aligned to <112> direction on the oxidized wafer by EB lithography. After shrinking of the resist pattern by O₂ ashing, a SiO₂ mask pattern is formed by RIE, and further narrowing of the SiO₂ pattern is performed with DHF. Then, a very narrow fin is formed by SOI etching in a tetramethylammonium hydroxide TMAH (2.38%) solution at 50 °C. TMAH is a well-known alkaline orientation-dependent etchant for a Si substrate in the field of the microelectromechanical system (MEMS) technology (23). The poly-Si gate is formed by the conventional RIE. After metallization, the device is sintered in a pure H₂ ambient at 400 °C.

Figure 5 (a) is the cross-sectional STEM image of the thinnest Si Fin we fabricated. From this STEM image, the ultra-narrow 13-nm-thick, 82-nm-high rectangular cross-section Si-Fin channel is confirmed. The aspect ratio of 6.3 is the highest among all
fins reported so far to our knowledge. It should be noted that the cross-section of the fin fabricated by the proposed orientation-dependent wet etching is perfectly rectangular. From the STEM picture of Fig. 5 (b), the ideal rectangular 5-Fins are confirmed. Figure 6 shows the I-V characteristics of the 13-nm-thick rectangular Si-Fin channel device. Here $I_d$ and $g_m$ are normalized by the effective channel width of 2 times fin-height to fairness. The gate length is 105 nm. The very high transconductance of 700 mS/mm, low sub-threshold slope of 73 mV/decade, and small drain-induced-barrier-lowering (DIBL) of 0.06 V are obtained. This high SCEs immunity and high drive current are typical double-gate properties as mentioned before. Figure 7 is the systematic $I_d-V_g$ characteristics of the fabricated devices as a function of the Si-Fin thickness. These experimental results excellently demonstrate that the
Fig. 6  (a) Drain current vs. gate voltage ($I_d$-$V_g$) and (b) drain current vs. drain voltage ($I_d$-$V_d$) characteristics for the 13-nm-thick rectangular Si-Fin DG MOSFET (FXMOSFET).
narrower Si-Fin is very effective to suppress the SCEs. The high suppression of the SCEs is owing to the double-gate device structure to shield the influence of the drain to the source. The S-slope becomes the almost ideal value of 64 mV/dec with reducing Si-Fin thickness to 13 nm. We can clearly conclude that the narrow Si-Fin thickness is very effective to suppress the SCEs. Figure 8 shows the electrical characteristics of the multi-Fin DG MOSFETs. The gate length is 365 nm. It is surprisingly notified that the ideal S-slope of 60 mV/decade is experimentally obtained even for the 5-Fins device. It is also noted from Fig.8 (b) that the drain current is exactly proportional to the number of Si-Fins. These distinct characteristics in Fig.8 are owing to the ideal rectangular cross-section fin channel.
Fig. 8  Electrical characteristics of the multi-Fin DG MOSFETs: (a) $I_D-V_g$ characteristic for a 5-Fins device with an ideal $S$-slope of 60 mV/dec, (b) $I_D$ vs. number of Si-Fins characteristic.
**Vertical-type DG MOSFET (IMOSFET)**

The second three-dimensional DG device is the vertical-type DG MOSFET using a newly developed process. The vertical-type DG MOSFET has strength of suitability with bulk Si and a weakness of fabrication. RIE conventionally used in the vertical channel fabrication has a lot of demerits, i.e., difficulty in thinning, RIE damage, causing rounded edge, and having no etch stopper (24-26). To overcome these difficulties, a novel process to fabricate an ultra-thin Si channel wall for a vertical DG MOSFET have been proposed by using the newly found ion-bombardment-retarded etching, IBRE (27, 28).

The main process flow of the vertical DG MOSFET by IBRE is shown in Fig.9. At first, we make a rough Si wall using a SiO₂ mask aligned to the <112> direction on a (110) Si substrate and the orientation-dependent wet etching in the TMAH solution. After removing the SiO₂ etching mask, we perform the ion implantation. Only the notched parts are ion-dosed. We found the ion-dosed region is hardly etched in the TMAH solution. We called this process as IBRE. Because the ion-dosed regions act as etch-stoppers in TMAH, the Si wall thinning can be carried out by re-dipping in TMAH. The SEM Si wall images after each step are also shown in Fig.9. It is noteworthy that a very narrow Si vertical channel wall is successfully obtained by the

![Diagram](image_url)
IBRE. After then, the ion-dosed regions are annealed and automatically become the source and drain. This unique process results in a gate-last process. The gate-last process is advantageous to introduce a high-K gate insulator material and a metal gate. Finally, a thin gate oxide is formed, followed by the gate electrode formation and SiO₂ CVD. The IBRE process possesses high bulk CMOS technology compatibility with the gate-last process, automatic formation of the source and drain.

The cross-sectional SEM image of the 15-nm-thick vertical DG MOSFET is shown in Fig.10. We call this “IMOS” from the resemblance of the cross-sectional shape of “T”. The IMOSFET in Fig.10 is the thinnest wall channel vertical DG MOSFET to our knowledge. Figure 11 shows the measured subthreshold $I_d-V_g$ characteristics of the fabricated n-channel IMOSFETs with the Si channel wall thickness $T_c$ as a parameter. It is clearly shown that the
subthreshold characteristics, e.g., the $V_a$ roll-off, S-slope, and DIBL, are drastically improved with decreasing channel wall thickness. The dependence of $V_a$ and S-slope on the channel thickness $T_c$ for the IMOSFETs is summarized in Fig.12. The experimental data for the fabricated IMOSFETs with a 15- to 64-nm-thick vertical channel are in good agreement with the simulation.

**Comments on low temperature use of DG MOS devices**

It is apparent from Fig.3 that the DG MOSFETs have a very small part of an active semiconductor region, i.e., an ultra-thin channel layer. It is concluded in the DG MOS devices that the ultra-thin Si channel between the two gates is very effective to suppress the SCEs. This device feature means that the DG MOSFETs may be robust against radiation damage in space use. The low temperature use of DG MOSFETs brings further advantage of low power operation. DG MOSFETs are characterized in nature by their steep subthreshold stand-on. This advantage is enforced in the low temperature operation. In other words, the very low power operation is possible at low
temperature. This property of DG MOSFETs is quite desirable in their space use. The source-drain series resistance of DG MOSFETs is a challenging issue for their low temperature use. However, the devices in space use may be replaced with DG MOSFETs instead of conventional bulk MOSFETs in future. It is considered that the DG MOS devices technology will be available soon.

SUMMARY

We are facing to the red brick wall for the further MOSFET scaling-down. For overcoming the difficulties, emerging double-gate (DG) MOSFETs are expected to be promising candidates for future ULSI circuits. Two types of DG MOSFETs, i.e., a Fin-type DG MOSFET (FXMOSFET) and a vertical DG MOSFET (IMOSFET) fabricated by the newly proposed processes are reported. The excellent device performance and short-channel effects immunity in these DG MOSFETs are experimentally confirmed. These DG MOSFETs should also be advantageous for low temperature space use. The wet-etching technology described here is promising for the successful fabrication of ultra-small DG MOSFETs. These emerging DG MOS devices will become available soon.

REFERENCES

New Insights on the Cryogenic Self-Heating of Silicon MOSFETs: Thermal Resistance of the Ceramic Package

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INVITED

ABSTRACT

The contribution to the total thermal resistance due to the ceramic package, used in most experiments to characterize the strong self-heating observed in MOSFETs operating at very low temperatures, has been determined as the dominant one for temperatures below 50K. The thermal properties of this ceramic, however, has never been reported. We present for the first time independent measurements of the thermal conductivity of a sample made of 90%-alumina from room temperature to liquid helium temperature. Typical commercial dual-in-line, high temperature, cofired, side-braze, ceramic packages were machined to produce free-of-parasitics samples, on top of which a serpentine-like metallic resistor was deposited. This resistor operated as both a thermometer and a heat source. The ceramic sample was mounted on the copper cold head of our open cycle cryostat, whereas the silicon diode thermometer located inside the cold head was used to calibrate the resistor when it was dissipating a very low power. Then D.C. measurements, at a much higher and thus heating power, were taken as a function of temperature. The thermal conductivity was extracted from the power vs. temperature difference across the geometrically well-defined sample. The thermal conductivity and thermal resistance of this ceramic package are presented, and their impact on the MOSFET’s self-heating is discussed.

I Introduction

At very low temperatures (LT) the behavior of the thermal properties of most solids differ qualitatively and quantitatively from that at room temperature (RT) [1]. Since the thermal conductivity ($\kappa$) and the specific heat decrease exponentially with the lowering of the temperature, it has always been believed that the self-heating (SH) becomes stronger under such conditions. It is also known that under deep cryogenic conditions not only several semiconductor physical parameters (charge carrier concentration, intrinsic con-
centration, mobility, diffusivity, generation/recombination lifetimes, among others), but also the transport mechanisms are strongly dependent on the operating temperature [2].

For instance, for non-degenerate and uncompensated Si samples, the dominant mechanism for impurity ionization at LT and low electric fields may be any of three different processes: shallow impact ionization, Poole-Frenkel or field-assisted thermal ionization and pure thermal ionization. For low electric fields, the dominance of the ionization mechanism changes abruptly in the short range of temperature from 4 K to 30 K [3].

Let us suppose that a non-degenerate n-type piece of Si at liquid helium temperature is suddenly biased with a 10-100 V/cm electric field. Instantaneously the device will operate as an insulator until the impurity ionization process starts, which will most probably be by impact ionization. Once the device is conducting, it will start generating heat, and given the low specific heat of Si at LT, this generated heat will lead to an important increment in the local temperature. Then the Poole-Frenkel mechanism of ionization will present with a further increase of the carrier concentration. This variation of the local temperature will also affect the carrier mobility, giving an additional contribution to the variation of current. The latter will affect the power consumption, thus a further variation of temperature will be expected. The local temperature will increase until the steady-state is reached due to the continuous transfer of heat through the Si substrate. At the beginning of this process, $\kappa_{th}$ has a very low value, promoting the device’s SH; as the temperature increases, however, $\kappa_{th}$ also increases and the substrate becomes more efficient in transferring heat, thus limiting the SH. After this transient, the steady-state temperature will be determined by the power consumption and the steady-state value of $\kappa_{th}$.

Thus, the study of the cryogenic SH of semiconductor devices becomes a fundamental issue since the localized variations of the device’s temperature importantly affects the operation under deep cryogenic conditions. In spite of the several experimental works regarding the cryogenic SH of Si devices, most of them focussed on bulk MOSFETs, little effort has been done in order to understand the actual origin of the measured temperature rise. The transient response to a voltage step has been used traditionally as a monitor for SH [4-6], regardless of the appropriateness of the assumptions on which this technique is based. In many cases, the transient response can be dominated by electrical rather than by thermal relaxation, leading to erroneous conclusions. A thermometer integrated in the same Si substrate has also been used to measure the actual temperature of a heating MOSFET located close to it [7,8]. The measured temperature rise was of the same order of magnitude as that obtained by using the transient approach. Nevertheless, these results did not explain the device’s thermal resistance expected from the point of view of geometries and material properties.

A more recent work [9] showed that the geometry-independent strong self-heating of integrated silicon devices cannot be due to the device-substrate system by itself. On the other hand, it is claimed that the main contributor to the observed high thermal resistances, among other thermal parasitics, should be the ceramic package used in most experiments. Nevertheless, there are no reports of the thermal properties of this ceramic material at cryogenic temperatures.
The aim of this work is to characterize thermally typical ceramic packages used to encapsulate MOSFETs for cryogenic applications. The earlier reports of cryogenic SH of Si MOSFETs are discussed in Sec. II, where several anomalies are addressed. The theoretical-experimental treatment presented in [9], whose results indicate that the thermal resistance of the ceramic package is mainly responsible for the strong SH of MOSFETs, are briefly reviewed in Sec. III. Finally, the fabrication and thermal characterization of the ceramic test structures are presented in Sec. IV, and the predicted thermal conductivity [9] is also compared to the measured one.

II Earlier measurements of cryogenic self-heating of MOSFETs

Since the first experimental studies on Ge and Si MOSFETs, Sesnic and Craig [4] suspected that the effective temperature of the active part of the device was much higher than the 4.2 ambient temperature. The main reason for such conclusion was the fact that the transconductance changed very little when the temperature was lowered from 77 K to 4.2 K, while a substantial change was observed in the 300 K - 77 K range. This saturation-like behavior of the transconductance, which is indeed affected by SH, is most likely due to the saturation of the mobility that may be determined by the neutral impurity scattering of carriers at LT. This scattering process depends weakly on temperature. Although their observations are unclear, their results are not too far from later experiments. Some of these measurements of SH in Si bulk MOSFETs are shown in Table 1.

<table>
<thead>
<tr>
<th>Device (Technique)</th>
<th>Device area (µm²)</th>
<th>Power (mW)</th>
<th>T_{amb} (K)</th>
<th>ΔT (K)</th>
<th>R_{th} (K/W)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-MOSFET (TDC)</td>
<td>760</td>
<td>30</td>
<td>20, 80, 200</td>
<td>24, 10, 9</td>
<td>800, 333, 300</td>
<td>[5]</td>
</tr>
<tr>
<td>p-MOSFET (TDC)</td>
<td>3143</td>
<td>46-60</td>
<td>20, 80, 200</td>
<td>24, 12, 11</td>
<td>522-400, 261-200, 239-183</td>
<td>[6]</td>
</tr>
<tr>
<td>n-MOSFET (IT@80µm)</td>
<td>49</td>
<td>120, 57, 32, 14</td>
<td>4.2</td>
<td>37, 32, 29, 25</td>
<td>308, 561, 906, 1786</td>
<td>[7]</td>
</tr>
<tr>
<td>n-MOSFET (IT@31µm)</td>
<td>24</td>
<td>40, 30, 15</td>
<td>4.6, 3.4, 1.7</td>
<td>115, 113, 113</td>
<td>[8]</td>
<td></td>
</tr>
</tbody>
</table>
In [4], Sesnic and Craig applied a steep risetime voltage step to the drain of an n-MOSFET, and the temporal change of the drain current was recorded. It was assumed that this change reflected the transient increase of the temperature of the channel. It was implicit that the thermal time constant, \( \tau_{th} \), of this device at such temperatures was much longer than any electrical relaxation time. Therefore, the initial drain current was taken as its value at the ambient temperature, \( I_{DS}(T=\text{amb}) = I_{DS}(t=0) \), as the SH had not yet started to increase the device's temperature. By taking this initial value for different ambient temperatures, a calibration curve \( I_{DS}(t=0) \) versus \( T_{\text{amb}} \) was obtained. The value of \( I_{DS} \) for a later time was taken as its value corresponding to the local temperature \( T = T_{\text{amb}} + \Delta T \), where the temperature rise \( \Delta T \) was time-dependent. The steady-state value of \( I_{DS} \) was recorded after the transient, and the corresponding \( \Delta T \) is the value shown in the first row of Table 1. Two different values for the thermal time constant were observed for two ranges of temperature: \( \tau_{th} = 1 \mu s \) at \( 4 \text{ K} < T < 40 \text{ K} \) and \( \tau_{th} = 10 \text{ ms} \) at \( 40 \text{ K} < T < 45 \text{ K} \).

A similar transient drain current (TDC) approach was used by Foty and Titcomb [5] for an n-MOSFET and by Foty [6] for a p-MOSFET. In both of these works, the authors characterized \( \Delta T \) for different power levels and for the wide temperature range of 20 K-200 K. A thermal time constant of the order of minutes was obtained regardless of the type of device, the ambient temperature and the power level. This \( \tau_{th} \) is five orders of magnitude longer than the value measured by Sesnic and Craig.

The TDC method may not be reliable since it is based on an incorrect assumption. Such heating transient must represent how long the heat generated in the MOSFET's channel takes to reach the heat sink (the bottom part of the Si substrate or the chip package), and not the heating of the channel. Actually, the device's temperature must increase sharply (because of the low value of the Si specific heat under deep cryogenic conditions) just after the voltage step is pulsed, and then must start decreasing as the heat is being transferred. In other words, the transient observed in [4-6] does not seem to be the result of heating but of the cooling of the channel. Hence, what the authors assumed to be \( I_{DS}(T = T_{\text{amb}}) \) was actually the value of \( I_{DS}(T = T_{\text{max}}) \), where \( T_{\text{max}} = T_{\text{amb}} + \Delta T(t=0) \).

A few years later, Gutierrez-D et al. [7] proposed the measurement of \( \Delta T \) in an n-MOSFET by using a diffused resistor acting as an integrated thermometer (IT); this resistor was built 80 \( \mu \text{m} \) away from the heating n-MOSFET. An integration time of 33 ms (assumed to be much longer than \( \tau_{th} \) at IT) was used at each D.C. operating point to ensure that the thermal steady-state was reached. Due to the 80 \( \mu \text{m} \) separation of the heater and the thermometer, an error of 12% was estimated for the measured \( \Delta T \).

De la Hidalga-W and Gutierrez-D [8] used a similar approach, where another n-MOSFET was used as a thermometer, instead of a diffused resistor, to measure the \( \Delta T \) of a heating n-MOSFET. In this case, the thermometer was located at 31 \( \mu \text{m} \) from the heater and the integration time for D.C. measurements was 20 ms; the measurements were conducted at 10 K.

In [7,8], the devices’ areas were one to two orders of magnitude smaller than those of the earlier works. Then, one would have expected a much higher \( \Delta T \) under comparable conditions of power dissipation and ambient temperatures. Nevertheless, that was not the...
case, as can be seen in Table 1. Furthermore, a direct comparison between the results in 
[7] and [8] reveals that the reduction of the device dimensions did not lead to a higher \( \Delta T \); 
on the contrary, a one-order-of-magnitude lower \( \Delta T \) was obtained for the smaller device. 
This could be due to the difference in the respective layouts; the thermometer of [7] was 
transverse to the MOSFET’s channel axis direction, or W-direction, while in [8], the ther-
nometer was along the L-direction. In addition, the thermometers were located at differ-
ent distances from the respective heaters.

It must be pointed out that a direct comparison of the cryogenic SH of MOSFETs 
shown in Table 1 has to be carefully interpreted. The thermal resistance of the device, \( R_{th} \), 
is determined by the geometry (substrate thickness, layout, chip cross section, dimensions 
of the integrated device, etc.), and the thermal properties of the materials involved in the 
final device (Si substrate; Al, W and/or Au for interconnections and bonding; polysilicon 
interconnections; glass for passivation; SiO2 for insulation; ceramic or plastic for packag-
ing; etc.). These different materials may form paths through which the heat can be trans-
ferred to the heat sink, all of them contributing to some degree to the overall \( R_{th} \), which is 
simply given by \( \Delta T/\text{power} \). Furthermore, one must take into account that under cryogenic 
conditions, the thermal properties of most solids strongly depend on temperature [1] and it 
is not possible to quantify their values for most of them. In addition, the particularities 
inherent to each experimental setup, which can introduce very different thermal loads or 
parasitics to the measurement of the SH, are additional reasons of such important dis-
agreements.

III Predicted Thermal Resistance of Si integrated devices

In 2000, De la Hidalga-W et al. [9] reported the calculated thermal resistance for a 
generic silicon integrated device, taking into account both, the precise geometries (for the 
silicon die as well as for the integrated device) and the well known silicon thermal con-
ductivity as a function of temperature. This device was fabricated using a 0.8 \( \mu \)m BiC-
MOS technology, and attached to a 24 pin dual-in-line side-brazed ceramic package (from 
NTK Technical Ceramics). The main body of this 1.5 cm x 3 cm x 0.1143 cm-thick pack-
age was made of 92%-pure black alumina. The 0.025 cm-thick lead frame was made of 
alloy-42 (Fe, 41% Ni, 0.8% Mn and 0.5% Co). Silver enriched conductive epoxy was 
used for attaching the Si die at the center of the package. The packaged chip was mounted 
in the cold-head of a closed cycle refrigerator and cooled to 5 K. The temperature was 
controlled by a Lake-Shore temperature controller, and D.C. measurements were taken 
with an HP 4145-B Semiconductor Parameter Analyzer.

The measured thermal resistance was obtained for the 5 K<T< 300 K range [9]; this 
thermal resistance is shown with symbols in Fig. 1-a). The two main contributors to \( R_{\text{Measured-Total}} \) the resistance due to the Si device, \( R_{\text{Device-Calculated}} \), and the resistance due to 
the ceramic package, \( R_{\text{Parasitic-Estimated}} \) are also shown. As expected, the thermal resis-
tance of the Si device follows the temperature dependence of the reciprocal of the silicon 
thermal conductivity, \( \kappa_{sh} \). It decreases with the lowering of \( T \) until a minimum is reached 
at \( \sim 30 \) K, corresponding to the maximum in \( \kappa_{sh} \), then it starts increasing sharply, corre-
spending to the sharp decreasing of silicon \( \kappa_{sh} \).
The $\kappa(T)$ of the poly-crystalline 92%-alumina could not be estimated since it strongly depends on the size of the grain and the devitrification process used to obtain it. Thus, the curve marked as $R_{\text{Parasitic-Estimated}}$ in Fig. 1-a) was obtained by simply using the relationship between these series resistances, $R_{\text{Measured-Total}} = R_{\text{Device-Calculated}} + R_{\text{Parasitic-Estimated}}$.

Under deep cryogenic conditions, the parasitic resistance dominated the measured incremental resistance of the device-package system. At temperatures around 300 K, both contributions were of similar magnitude. However, as the temperature reduces below 100K, the package resistance becomes much more dominant. This also explained the lack of a position dependence of the temperature rise at LT and an observable though weaker position dependence at higher temperatures.

By neglecting other possible contributions to $R_{\text{Parasitic-Estimated}}$, such as the chip-package and the package-cold-head interfaces, whose values are very difficult to determine for the wide temperature range under consideration, the $\kappa(T)$ of the 92%-alumina was estimated. A similar relation to that used to calculate $R_{\text{Device-Calculated}}$, but using the geometrical features of the package-chip system (where the whole chip is now considered as the heat source), was used to extract the geometrical factor from $R_{\text{Parasitic-Estimated}}$ to obtain the $\kappa(T)$ shown in Fig. 1-b). Since in the literature there are no reports on the tempera-
tured, dependence of the 92%-alumina $\kappa_{th}$, then the results are compared to that of 96%-alumina [10] and 99.9%-alumina [1]. In addition to the lack of data for alumina with 92%-purity, the $\kappa_{th}(T)$ of poly-crystalline aluminas can present a wide span in values [1], mostly in the LT range. Nevertheless, the expected behavior of $\kappa_{th}$ for a less pure and noncrystalline alumina is a reduction in the maximum (due to the increased defect density) and a rightward shift of that maximum, due to the decreased mean free path for phonon scattering by diffused boundaries.

The other contributions to $R_{\text{parasitic}}$ were more difficult to estimate. The chip-to-package contribution depends not only on the thermal conductivity of the epoxy but on its uniformity and thickness. The thermal properties of the epoxy are well known for temperatures around RT and above; however, as in the case of the package’s ceramic body, they have not been characterized at LT. The fact that die attaching is performed by hand, affecting the uniformity and thickness of the layer that introduces higher complications for the estimation of this contact resistance. Additionally, between the Si chip and the ceramic body there is a conducting layer made of alloy-42; this layer does not introduce an important contribution by itself (it is around ten times thinner than the ceramic body whereas its thermal conductivity is similar) but introduces two more interfaces that may increase the overall contact resistance. The contribution of the package-to-cold-head contact resistance must be less important as there is an intimate contact between larger surfaces. An indium-based grease is normally used to improve this contact. Nevertheless, as in the case of the epoxy, this grease has not been characterized at low temperatures.

The estimation of $\kappa_{th}(T)$ for the ceramic body of the package in Fig. 1-b) must be taken with great care, since several unknown contributions have been neglected. The predictable $\kappa_{th}(T)$ of Si, which is a crystalline, very pure and thoroughly characterized material, contrasts with that of the other materials involved in an encapsulated IC. Unfortunately, the results shown in Fig. 1-a) dictate that the strong cryogenic SH observed for the Si generic device was totally determined by the non-silicon components of the encapsulated IC. This also explained why the experimental data of Table 1 led to thermal resistances that did not depend on the geometry of the MOSFETs.

IV Thermal characterization of the ceramic package

A 48 pins dual-in-line high temperature cofired side-brazed ceramic package, manufactured by KYOCERA, and made of 90%-pure black alumina ($\kappa_{th}=0.18 \text{ W/cmK at } 300\text{K}$, according to the manufacturer) was used in this experiment. It is worth mentioning that the NTK ceramic package used in the 2000’s experiment was very similar but made of 92% alumina, with a reported $\kappa_{th}=0.17 \text{ W/cmK at } 300 \text{K}$ [9]. A serpentine-like metallic resistor (heater-thermometer) was deposited on the top surface of a machined section of these ceramic packages, using three different metals: Aluminum, Nickel, and Titanium with a thickness of 2000 Å, 5000 Å, and 9000 Å, respectively. As sketched in Fig. 2, the serpentine resistors were composed of thirty 300-μm-width lines with a 100 μm-pitch, covered about 60% of the ceramic surface, simulating a uniform metallic plate. The correction factor was estimated to be less than 10%. All but 4 pins were removed to minimize thermal parasitics, and they were wire bonded to the terminals of the serpentine in order to conduct 4-probes measurements of the resistances. Photographs of the test structures are
shown in Fig. 3. In actual test structures, the ceramic samples were machined to the final dimensions before e-beam evaporating the metallic films and patterning the resistors using a lift-off technique.

FIGURE 2: Schematic (not to scale) showing the relevant dimensions of the ceramic sample with the deposited metallic resistor on its top surface. The two terminals of the serpentine were wire bonded to the remaining 4 pins in a Kelvin configuration.

FIGURE 3: Photographs of the test structures before removing most of the pins: a) before cutting the ceramic sample, and b) after machining the sample. The metallic serpentine resistor can be seen on the top of the sample.
The three samples were mounted in the cold-head of an open cycle refrigerator and cooled to 4.2 K. Care was exercised in order to avoid any heat transfer mechanism other than heat conduction from the top surface of the ceramic sample to the cold head of the cryostat. The vacuum chamber was evacuated to less than 10 microns, and a radiation shield was also mounted. The temperature was controlled using a Lake-Shore temperature controller, and the D.C. I-V measurements were taken with an HP 4155-B Semiconductor Parameter Analyzer, using an integration time longer than 20 ms to guarantee that the thermal steady-state was reached for each operating point. The experimental setup is shown in Fig. 4.

![Cross Section View](image)

**FIGURE 4:** Experimental setup showing a cross section view of the vacuum chamber, the cryostat, and the mounted sample.

By measuring the resistance at very low power levels (of the order of tens of nW) the calibration curves for the test structures were obtained; they are shown in Fig. 5-a) together with their relative sensitivity as a function of the ambient temperature, Fig. 5-b). The Nickel structure showed a higher sensitivity in most of the measured temperature range, then it was chosen as the sample under study. However, it is important to mention that the measured thermal resistance behaved fairly similar among the three samples tested in this experiment. The calibration curves show that all the resistances tend to satu-
rate at very low temperatures giving rise to very low sensitivities. Accordingly, we are reporting results only for temperatures above 20 K. In order to extrapolate measured temperatures on top of the ceramic samples, low order polynomials were fitted to the experimental calibration curves.

![Graphical representation of calibration curves and relative sensitivity versus ambient temperature for the three fabricated test structures.](image)

**FIGURE 5:** a) Calibration curves and b) relative sensitivity versus ambient temperature for the three fabricated test structures.

Because of the low sensitivity of these resistors, a higher power had to be applied to the heating structures to obtain a significative $\Delta T$. The measured $\Delta T$ versus power curves, with the ambient temperature as a parameter, are shown in Fig. 6 for the Nickel structure. These curves are compared to those reported in the 2000's experiment [9] in the same figure. It can be seen that the behavior of the $\Delta T$-power curves is quite similar for both experiments, though the scales are quite different. The quantitative differences are just due to the geometrical factors involved in the ceramic samples, as well as the contribution to the total thermal resistance arising from the presence of the small silicon die in the 2000's experiment. In both set of curves one can see that the self-heating, and thus the thermal resistance, increases as the ambient temperature decreases. The temperature rise presents a fairly linear behavior at temperatures around 300 K, which is consistent with a slow decreasing thermal conductivity for an increasing local temperature, while a saturation-like behavior can be appreciated as the ambient temperature is further reduced. This phenomenon is ascribed to a sharply increasing thermal conductivity as the local temperature increases.
From these $\Delta T$-power curves, the thermal resistance of the ceramic sample, defined simply as $\frac{d\Delta T}{d\text{Power}}$ was obtained as a function of the ambient temperature. The results are shown in Fig. 7-a), where the thermal resistance of the new structure is plotted using filled triangles, while the line and the other symbols belong the 2000's experiment. We can see an important disagreement between the estimated parasitics (ascribed to the ceramic package) and the direct measurement of the thermal resistance at temperatures above 77 K. This is mainly due to the different geometries and the contribution of the silicon die in the 2000's experiment. In order to obtain a correct comparison between the results of these experiments, the geometrical factors have to be eliminated, and a thermal conductivity must be extracted; the results are shown in Fig. 7-b).

There is a good agreement in the thermal conductivities at room temperature, with a slightly higher $\kappa_{th}$ for the KYOCERA ceramic sample (90%-alumina) than the estimated $\kappa_{th}$ from the NTK sample (92%-alumina), which agrees somewhat with the value interpolated from the data provided by the manufacturers. The values shown in Fig. 7-b) at 300 K, however, are about half of the values of $\kappa_{th}$ for the two levels of alumina purity. It is necessary to point out that the $\kappa_{th}$ reported by manufacturers refers to the polycrystalline raw alumina, before the fabrication of the ceramic package. The fabrication process must alter importantly such values since the final package, which is the material under characterization, is composed of several layers of some refractory metals placed between layers of alumina coming from a slurry that also contains not only aluminum oxide (alumina) but
also some other materials such as silicon oxide and calcium oxide. Once the stacked multilayer structure is complete, it is sintered at a high temperature (typically 1600 C); finally, the metallic pins are attached to the sides of the package. This multilayer nature of the body makes unreal to define a \( \kappa_{th} \) for the sample; actually this parameter is a function of the position across the sample. The \( \kappa_{th} \) we are reporting must be regarded as the averaged value of the position dependent \( \kappa_{th} \).

As can be seen in Fig. 7-b), the dependence on temperature of the \( \kappa_{th} \) for the sample used in the present experiment is that expected for a non-crystalline material; it also shows a plateau, for temperatures between 100 K and 200 K, which is typical for glasses [1]. For deep cryogenic conditions, that is below 77 K, \( \kappa_{th} \) decreases sharply with the lowering of the temperature, thus giving rise to such strong cryogenic self-heating observed in encapsulated MOSFETs. Thus, the thermal resistance of the ceramic package dominates the total resistance of the encapsulated device, especially at temperatures of liquid helium, giving rise to a cryogenic self-heating independent on the MOSFET geometry, which agrees with the reported results shown in Table 1.

![Graphs](image-url)  
**FIGURE 7:** a) Comparison of the thermal resistance of the ceramic sample with the parasitics reported in [9], and b) comparison of the thermal conductivities. Direct Measurements is the result from the present experiment.
V Conclusions

The cryogenic behavior of the thermal conductivity of a typical ceramic package has been reported for the first time. A high temperature cofired side-braze dual-in-line ceramic (90%-alumina) package made by KYOCERA, was used as the material whose thermal conductivity was obtained for the 20 K < T < 300 K range. A geometrically well defined test structure was fabricated in order to avoid any correction factor and also to assure a one-dimensional heat transport. The obtained thermal conductivity depends on temperature similarly to that of noncrystalline materials, such as glasses, presenting a plateau in the 100 K < T < 200 K range, and decreasing sharply as the temperatures decreases to liquid helium temperatures. The room temperature value of the thermal conductivity was about half of the value reported by the manufacturer for the raw material, which is a powder made of 90%-pure polycrystalline alumina. Evidently, the fabrication process as well as the incorporation of other material in the starting slurry, plus the addition of metallic layers, which also leads to thermally resistive interfaces, give rise to a detrimental effect on the final value of the averaged thermal conductivity of this ceramic. Finally, the very low values of the thermal conductivity, hence a high value of the thermal resistance of the ceramic package, fully explain the geometrically independent strong self-heating reported for MOSFETs operating under deep cryogenic conditions.

VI Acknowledgments

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VII References


HIGH-SPEED CONVERSION OF PICOSECOND, MILLIVOLT PULSE SIGNALS TO CMOS VOLTAGE LEVELS

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ABSTRACT

Among the situations that require high-speed interfaces between superconductor circuits carrying millivolt single-flux-quantum (SFQ) pulses and volt-level semiconductor circuits are drivers for room-temperature or intermediate-temperature semiconductor circuits and interfaces between SFQ logic and a proposed hybrid Josephson-CMOS memory. The particular focus of this paper is on the latter application, in which case, the principal concern is the switching delay. We are reporting developments on a previously proposed hybrid Josephson-CMOS interface amplifier and evaluating a possible alternate approach. The hybrid circuit employs a series array of 400 Josephson tunnel junctions as a load on an NMOS driver. We will report calculations of the effect of parasitic inductance and capacitance associated with the load array on the amplifier switching delay. Also, a cryogenic CMOS amplifier circuit will be discussed for comparison with the hybrid amplifier.

INTRODUCTION

Some complimentary features of semiconductor and superconductor technologies suggest that their combined use could be advantageous in applications. The metallic superconductors based on niobium and its alloys and compounds require operation at temperatures of 10 K or less. Some semiconductor devices such as MOS transistors work well at those cryogenic temperatures; in fact, better than at 300 K.

There is a large difference in energy levels of the signals in the two technologies. The superconductor energy gap is on the order of millivolts and semiconductor gaps are on the order of volts. Signal voltage levels have a corresponding discrepancy, and that places a significant burden on interfacing between the two technologies.

One particular application of a combined semiconductor-superconductor hybrid is of great importance. Superconductor digital circuits in the form of single (magnetic) flux quantum logic have been shown to offer speeds in the range of 50-100 GHz. The currently popular rapid single-flux-quantum (RSFQ) logic circuits have been extensively...
studied and many circuits have been demonstrated, some at speeds exceeding 50 GHz [1, 2].

There has, however, been no wholly superconductor memory system of sufficient size to provide the memory needed for Josephson digital system applications. We have proposed a solution using the core of a CMOS memory, operated at 4 K, with Josephson superconductor peripheral circuits, including bit-line detectors and input interface circuits. [3, 4, 5] The latter, which must amplify the millivolt, picosecond, single-flux-quantum pulses to volt levels to drive the CMOS decoder circuits, is the subject of this paper. The very high density memory achieved in MOS technology is especially desirable.

JOSEPHSON TECHNOLOGY

Josephson junctions are the active elements in superconductor electronics. [6] The most used configuration is the sandwich structure shown in Fig. 1a, in which the barrier is a thin (~ 1 nm) oxide layer separating two superconductors. A highly developed thin-film technology based on a trilayer of Nb/AlO_x/Nb, which covers an entire wafer, is etched to pattern the Josephson junctions. (Si wafers are used for convenience to allow application of existing fabrication tools.) Niobium thin-film integrated circuits are built around these junctions. The I-V characteristic is shown in Fig. 1b. By shunting the junction with a small resistor, the combined I-V characteristic is that shown in Fig. 1c; this is the type of characteristic needed for single-flux-quantum logic circuits.

Most research today in superconductive digital circuits is focused on the use of RSFQ circuits in which the signals between gates are picosecond pulses of voltage amplitude somewhat less than 1 mV. In superconductivity, magnetic flux is stored in units of the flux quantum, \( \Phi_0 = 2.07 \times 10^{-15} \) Wb; flux passing through any closed superconducting loop must contain a multiple of the flux quantum. RSFQ circuits (see Fig. 2) store single flux quanta and pass corresponding voltage/current pulses between gates. The circuits comprise shunted Josephson junctions designated by \(-x\)-, inductors, and supply- current resistors (the \( I_b \) currents are dc). The inductors are typically on the

![Fig. 1](image-url)

(a) Josephson tunnel junction. (b) Josephson tunnel junction I-V characteristic. (c) I-V characteristic of a tunnel junction combined with a small shunt resistor.
order of a few picohenries and are simply short sections of microstrip line. Fig. 2 shows representatives of unclocked and clocked RSFQ circuit components. The time integral of

![Diagram](image)

Fig. 2 (a) A pulse splitter as a representative of the set of unclocked circuits used as parts of RSFQ gates. (b) RSFQ gates are individually latched; this set-reset flip flop is representative of the latches incorporated in RSFQ gates.

the voltage pulses passed between these circuits equals one flux quantum, so the energy per bit is on the order of $10^{-19}$ joules. (There is an additional static power dissipation in the supply resistors for the dc currents.) Higher current densities in the junctions lead to shorter pulses and therefore allow higher clock rates. As an example, the fabrication line at Northrop Grumman Space Technology currently makes highly controlled junctions with 8 kA/cm² current density and they have experimental studies on 20 kA/cm² junctions. [7] The former should be sufficient for circuits with >50 GHz clock rates.

HYBRID MEMORY

The focus of the present research is on an amplifier to interface the RSFQ logic circuits to the CMOS decoder of a 64-kbit semiconductor random access memory (RAM). The system is shown in Fig. 3. The memory cells are the 3-transistor DRAM type cells; there is negligible leakage because of carrier freeze-out so it is possible to operate the memory without refreshing, i.e., as though it were a static RAM. The bit-line currents are detected by near-zero-input impedance, extremely sensitive and high speed Josephson circuits. The OR/MUX function will be made with high-speed Josephson circuits. The most difficult problem is the input interface amplifiers.
Fig. 3 Hybrid Josephson-CMOS memory unit. The input interface circuits at the left side must amplify the RSFQ millivolt, picosecond pulses to volt levels for the CMOS decoders.

**INTERFACE AMPLIFIER**

The main challenge for the input amplifier is a short delay. The entire access time between the address input and the data output must be less than 1 ns. A large fraction of that will be used in the semiconductor parts (decoder and bit-line delay). We are targeting 100 ps for the maximum delay in the input amplifier. The candidate circuit is shown in Fig. 4; we have studied separately the parts numbered 1 and 2. For the calculations on the circuit in Fig. 2 that are reported here, the Josephson junctions are assumed to use a current density of 6.5 kA/cm² and the transistors are 0.25 µm CMOS made by National Semiconductor (NSC). Part 1 of the amplifier comprises circuits that have been well evaluated in other situations; we are assuming that our simulations, which give a total delay for Part 1 of 22 ps, are sufficiently accurate.

Part 2 is the more novel circuit. Low-frequency functionality experiments have been run; we find that with 40 mV input, the output can be a large fraction of a volt, and therefore sufficient to drive the decoder. Simulations of that part of the circuit depend strongly on the parasitic capacitance (represented by C₀ in Fig. 4) between the 400-Josephson junction array and ground, and to some extent on the parasitic inductance of the array. We have considered (in calculations) various ways of reducing the parasitic capacitance. One is to enlarge the gap between the ground plane and the edge of the array. Another is to etch a deep trench in the substrate around the array. A third is to lay
out the array in a spiral form rather than a serpentine and connect the load end of the array (location of $C_0$) at the center and, therefore, further away from the ground plane. A more radical but much more effective approach is to etch from the back of the chip leaving only a 1 μm membrane under the array. We calculated $C_0$ for these different alternatives and performed simulations of the switching delay. We estimated the inductance of the serpentine and spiral array configurations. The simulations of the switching of the circuit in Part 2 with these parasitic inductances indicate that they are not as important as the parasitic capacitances.

Summarizing the simulations of the Part 2 circuit, we can estimate that without thinning the substrate, the other parasitic reduction techniques will lead to a delay of about 65 ps. The use of the thinned substrate will give a delay of 38 ps.

In order to do the simulations of the Part 2 circuit, it is necessary to have a model for the MOS devices at 4 K. The NSC 0.25 μm devices, Rohm 0.35 μm MOSFETs, and Hitachi 0.18 μm devices have all been modeled for these and similar calculations. The manufacturer's 300 K models have been used with parameters chosen to get the best fit to the 4 K I-V characteristics. We are in the process of getting improved data on the output
capacitances at that temperature. Preliminary results show that low temperature capacitance drops, so the simulation results using 300 K capacitance values are conservative.

Taking into account the delays in the two parts of the circuit, we can expect delays of between 60 ps and 90 ps, depending on which choices we make in reducing the parasitic capacitance. It seems that it will not be difficult to achieve the targeted subnanosecond access time for the 64-kbit memory.

We have also considered using a completely CMOS version of the Part 2 circuit. Simulations of an optimized cascaded differential-transconductance amplifier, if fabricated in the Hitachi 0.18 μm CMOS process, would have yielded a delay of 71 ps. This new result for delay is similar to that of the circuit with the 400-junction load; it is much simpler and will be considered as an alternative.

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REFERENCES

OPERATION OF DOUBLE GATE GRADED-CHANNEL TRANSISTORS AT LOW TEMPERATURES

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ABSTRACT

This work studies the use of graded-channel profile on double gate SOI MOSFETs from room temperature down to 95 K with the aim of studying the analog performance. Two-dimensional simulations are performed to provide a physical explanation for the improved analog device characteristics given by the double gate graded-channel MOSFETs. It is demonstrated that double gate graded-channel MOSFETs can provide extremely improved Early voltage, high transconductance and drive current in comparison to the conventional double gate fully depleted SOI MOSFETs with similar dimensions. A degradation in the Early voltage as the temperature decreases has been found but this reduction reflects negligibly in the low frequency open loop gain for a temperature range of 150 K to 300 K due compensation provided by the transconductance to drain current ratio.

INTRODUCTION

The extreme scaling of MOSFETs faced in the past few years lead to a great interest in double gate (DG) transistors because they can provide better scaling properties in comparison to conventional single gate (SG) devices, allowing smaller dimensions without suffering short-channel effects [1]. Electrical characteristics such as quasi-ideal subthreshold slope, large transconductance, high current drive capability and possible volume inversion made the DG MOSFET a very attractive structure in comparison to SG transistors[2-3]. As one of the proposed double gate architectures, the Gate-All-Around (GAA) [4] structure, on which the channel region is surrounded by the gate oxide and metal electrode, has presented excellent analog behavior in extreme high-temperature and radiation environments [5] with the advantage that the process flow of conventional fully depleted (FD) SOI MOSFETs is easily accommodated.
Regarding the analog operation of MOSFETs, as the device dimensions shrink, the reduction of the intrinsic gain due to the Early voltage lowering is a major problem that must be addressed properly. To overcome this issue, the use of asymmetric channel devices has been suggested both in bulk [6-9] and SOI [10-15] technologies. In all these structures the channel region presents higher doping level in the source side than in the drain side.

Among these solutions, results reported for SG graded-channel (GC) SOI nMOSFETs in comparison to conventional SOI nMOSFETs show increased drain breakdown voltage, transconductance and reduced output conductance for equal channel length (L) [13-16]. In this transistor the natural wafer doping level is kept in the drain side of the channel, while the threshold voltage ionic implantation is performed only in the source side. As a first approximation, this low doped region can be interpreted as an extension of the drain below the gate (through the inversion layer) and the device effective channel length \(L_{\text{eff}}\) is almost equal to \(L-L_{\text{LD}}\), where \(L_{\text{LD}}\) is the length of the low doped region [13]. This approach differs from the previously mentioned ones since it is fully compatible with the conventional processing of fully-depleted SOI MOSFETs, with no additional steps, and since the drain region is kept undoped. Previous works on single gate graded-channel SOI nMOSFET showed largely improved Early voltage, high transconductance and reduced die area for identical frequency of operation [15].

The first results on graded-channel GAA transistors have been presented at room temperature in [17] where impressive Early voltages in the range of 1000 V^{-1} for a 2 μm long transistor have been presented, by far outperforming any previously reported values for this channel length.

The temperature reduction constitutes an interesting way of improving the device performance due to the increased minority carrier mobility and velocity saturation, reduced inverse subthreshold slope and junction capacitances, finally resulting in better switching characteristics than at room temperature without scaling the device dimensions [18].

In this paper we present the impact of the GC architecture on GAA devices regarding analog circuit design in the temperature range of 300 K down to 95 K. Experimental results and two-dimensional simulations are used to support the analysis.

**FABRICATION PROCESS DESCRIPTION AND EXPERIMENTAL RESULTS**

Conventional (i.e. uniformly doped from source to drain) and GC GAA transistors have been fabricated simultaneously, starting from an p-type Unibond material with concentration of about \(10^{19} \text{ cm}^{-3}\), according to the process described in [5]. The final thicknesses of the gate oxide, silicon film and buried oxide are 30 nm, 80 nm and 390 nm, respectively. After the threshold voltage adjust implantation a p-type doping level of about \(10^{17} \text{ cm}^{-2}\) is obtained. As previously mentioned, this implantation is masked in the drain side of the channel and the remaining channel region keeps the wafer doping level. Devices with 3 parallel fingers were made, each one with \(L=3 \mu\text{m}\) and \(W=3 \mu\text{m}\) (\(W\) being the channel width). In case of GC GAA, several combinations of the ratio \(L_{\text{LD}}/L\) (\(L_{\text{LD}}\) is...
the length of the unimplanted region) were designed. Figure 1 presents the cross section of the GC GAA transistors.

Figure 1 - Cross section of the Graded Channel GAA SOI nMOSFET.

To perform the measurements the devices were cooled down to 95 K and after the temperature stabilization the measurements were performed using a HP4156C semiconductor parameter analyzer. All the devices have been measured starting from the lowest temperature (95 K) up to the room temperature.

The most important figures of merit regarding the analog device performance are the low-frequency open-loop gain ($A_{V0}$) and unity-gain frequency ($f_t$), classically described as [19]:

$$A_{V0} = \frac{g_m V_{EA}}{I_{DS}}$$

(1)

$$f_T = \frac{g_m}{2\pi C_L}$$

(2)

where $I_{DS}$ is the drain current, $g_m$ is the transconductance, $V_{EA}$ is the Early voltage and $C_L$ is the load capacitance.

Figure 2 plots maximum transconductance evolution as a function of the temperature for the measured GC GAA transistors. Due to the effective channel length reduction provided by the low doped region, the peak transconductance increases as the length $L_{LD}$ is increased. There is a practically linear increase of the maximum $g_m$ as the temperature reduces, independently of the low doped region length. This larger transconductance as the temperature reduces is related to the carrier mobility increase as a
function of the temperature lowering[18]. From the analog operation point of view, this increase of $g_m$ works favorably to increase $f_T$ (equation 2).

Using equation (1), the analysis of $A_{\omega 0}$ has been partitioned in two parts, firstly looking at the $g_m/I_{DS}$ ratio as a function of the temperature. Figure 3 presents the experimental $g_m/I_{DS}$ curves as a function of the normalized drain current $I_{DS}/(W/L_{eff})$, extracted for the GC GAA with $L_{LD}/L=0.2$ at different temperatures and with $V_{DS}=1.5$ V.

Figure 2 – Maximum transconductance against temperature for GC GAA MOSFETs.

Figure 3 – Measured $g_m/I_{DS}$ ratio as a function of the scaled drain current for the GC GAA transistor with $L_{LD}/L=0.20$ in the temperatures of 150 K, 200 K and 300 K.
The maximum $g_m/\lambda_{DS}$ is reached in weak inversion regime and is classically expressed by equation (3)[19]:

$$\frac{g_m}{\lambda_{DS}} = \frac{q}{n_{wi}kT}$$

where $S$ is the inverse subthreshold slope, $q$ is the electron charge, $k$ is the Boltzmann constant, $T$ is the absolute temperature and $n_{wi}$ is the body factor in weak inversion.

Double gate transistors are known to have nearly ideal $g_m/\lambda_{DS}$ ratios (around 38 V⁻¹ at room temperature) due to the excellent channel control, leading the body factor very close to the unity[5]. However, in fig. 3, the weak inversion regime is dominated by a parasitic lateral transistors, i.e. along the edges of the active area, as indicated by the hump seen between moderate and strong inversion regimes. The maximum $g_m/\lambda_{DS}$ does then not achieve the theoretical values linked to the main channel analysis.

As the temperature decreases there is an increase in the maximum $g_m/\lambda_{DS}$ ratio thanks to the direct influence of the temperature in equation (3). However, this increase is attenuated by the presence of interface trap densities that degrade the term $n_{wi}$ in low temperatures, as expressed by equation (4)[20]:

$$n_{wi} = \left(1 + \frac{C_{it1}}{C_{oxf}} + \frac{C_{it2}}{C_{oxb}}\right) - \frac{C_{si}}{C_{oxf}} - \frac{C_{si}}{C_{oxb}}$$

where $C_{si}$ is the silicon film capacitance per unit of area, $C_{oxf}$ and $C_{oxb}$ are the front and back oxide per unit of area, $C_{it1}$ and $C_{it2}$ are the capacitance of the interface trap densities per unit of area at the front and back interface, respectively.

The degradation in $n_{wi}$ is caused by the increase of $C_{it1}$ and $C_{it2}$ as the Fermi level approaches for the Bandgap edges in low temperatures, where the interface trap density is generally larger than close to the midgap [21].

The most important implication of the $L_{LD}/L$ increase is the reduction on the threshold voltage ($V_{TH}$) caused by the charge sharing below the gate. The $V_{TH}$ reduces from 0.3 V for conventional and GC GAA with $L_{LD}/L=0.2$ down to 0.25 V for GC GAA with $L_{LD}/L=0.5$ at room temperature.

Figure 4 shows the $I_{DS}$ against $V_{DS}$ curves, extracted at a gate voltage overdrive ($V_{GF}=V_{GF}-V_{TH}$) of 200 mV for the fabricated GC GAA nMOSFETs at room temperature and at 95 K. Varying the ratio $L_{LD}/L$ an almost linear increase in the saturation current versus $L-L_{LD}$ is observed.
From the $I_{DS} \times V_{DS}$ curves measured at several temperatures the $V_{EA}$ has been extracted by using a linear regression in the range $0.75 \leq V_{DS} \leq 2.0 \text{ V}$ and the obtained results as a function of the temperature are presented in figure 5. The Early voltage measured for conventional GAA at 300 K is 69 V. It becomes maximum in GC MOS with $L_{4D}/L = 0.2$ and decreases with temperature decrease.

Figure 5 – Extracted $V_{EA}$ for GC GAA transistors as a function of the temperature.
Using the experimental data for \( g_m/\text{IDS} \) and \( V_{\text{EA}} \) at \( V_{\text{GT}} = 200 \text{ mV} \), for each \( L_{\text{LD}}/L \) ratio, the \( A_{V_0} \) has been calculated and the obtained results are plotted in figure 6 as a function of the temperature reduction.

![Figure 6](image)

**Figure 6** – Calculated \( A_{V_0} \) as a function of the temperature for GC GAA transistors.

In the range of \( L_{\text{LD}}/L \) between 0.20 and 0.35 the gain is around 90 dB and does not suffer a large variation at low temperatures down to 150 K. In spite of a severe reduction of \( V_{\text{EA}} \) in low temperature, this reduction is compensated by the increase of \( g_m/\text{IDS} \), leading to a weakly temperature-dependent \( A_{V_0} \) with less than 10% reduction in the range of 300 K down to 95 K. Similarly, for the GC GAA with \( L_{\text{LD}}/L \) equal to 0.50 the reduced \( V_{\text{EA}} \) results is a gain of 80 dB, which is reduced to about 72 dB at 95 K. Even in this case, there is no strong temperature variation on \( A_{V_0} \). The calculated gain of the conventional GAA at room temperature is 67 dB, being smaller than of any GC GAA transistor in all temperature range.

In the presented analysis no self-heating effects affecting the results have been observed, even at 95 K, as DG transistors are less subjected to this effect [22] and the applied gate voltages have not been large enough to induce such an occurrence.

**DEVICE PHYSICS AND DISCUSSION**

In order to define the physical reasons for the improved \( V_{\text{EA}} \) in GC devices, two-dimensional simulations [23-24] were performed in 1\( \mu \)m long conventional and GC GAA with \( L_{\text{LD}}/L \) equal to 0.25 and 0.50 transistors at 100 K. Models accounting for the electric field dependent carrier mobility with velocity saturation, SRH recombination/generation
with doping-dependent lifetime, Auger recombination, bandgap narrowing, and impact ionization with electric field were included in the simulations. Default simulator coefficients for all parameters have been employed with no optimization which is beyond the scope of this physical analysis and may affect the quantitative results but not the qualitative analysis and trends.

Figure 7 presents the resulting $I_{DS}$ curves obtained against $V_{DS}$ with and without the impact ionization model and the impact ionization (I.I.) rate (defined as I.I./$I_{DS}$).

![Figure 7 – Simulated drain current and impact ionization rate for conventional and GC GAA transistors with $V_{GT}=200$ mV and operating at 100 K.](image)

The presence of a low doped region reduces the drain-to-channel pn junction potential barrier and the peak electric field near the drain, directly affecting the amount of impact ionization current, as clearly expressed in figure 7. Both GC GAA structures present very reduced impact ionization rate in comparison to conventional GAA transistor. Increasing the length $L_{AD}$ there is an increase in the drain saturation current which causes a minor increase in the impact ionization current. Although there is a difference in the impact ionization rate between conventional and GC GAA structures, the total contribution of I.I. current does not exceeded 10 % indicating that the dominating influence for the observed $V_{BA}$ increase is weakly related to I.I. mechanism for drain bias smaller than 1 V, as clearly observed in the plotted $I_{DS} \times V_{DS}$ curves neglecting the impact ionization. Prior to the region where the I.I. phenomenon becomes important, i.e. for $V_{DS}<1$ V in conventional GAA, the curves with and without I.I. coincide indicating that the Early voltage is being dominated by the channel length modulation due to the drain bias. As the drain voltage is increased, the action of the parasitic bipolar structure becomes important and degrades the analog performance in two ways: $V_{BA}$ reduction and limitation of the output swing.
The potential distribution along the channel extracted at a gate voltage overdrive of 200 mV for applied drain bias of 1.0 V and 2.0 V is plotted in figure 8. The dotted lines indicate the low doped region limit for each GC transistor.

![Simulated potential distribution](image)

Figure 8 – Simulated potential distribution along the channel position for the conventional and GC GAA transistors at $V_{GT}=200$ mV.

In the conventional GAA transistor, as the $V_{DS}$ is increased the channel length modulation can be observed in figure 8 by the penetration of the applied drain bias to the channel region. On the other hand, it is possible to see that practically all the $V_{DS}$ increase is absorbed in the low doped region of all GC GAA transistors and do not affect the "main" device channel (high doped region) resulting in the extremely reduced drain output conductance and consequently the higher Early voltage.

Due to the improved $V_{EA}$ one can see that the GC GAA can provide very high gain operational amplifiers. In GC GAA devices the effect of the channel architecture improves $V_{EA}$ for $L_{dd}/L$ smaller than 0.3. Although for the larger ratios, the impact ionization tends to degrade $g_6$, the resulting $V_{EA}$ is always larger than in conventional GAA.

CONCLUSION

This paper critically discussed the enormous potential of double gate graded-channel fully-depleted SOI nMOSFET for high performance analog circuits from room temperature down to 95 K by looking to the key analog design parameters: the open loop gain and transition frequency.
The use of double gate graded-channel devices allows for realization of very high-gain operational transconductance amplifiers with improved unity gain frequency for similar $L$.

The impact ionization rate due to the high electric field close to the drain is efficiently reduced and an extremely improved Early voltage is obtained since the potential variation in the drain is practically totally absorbed in the low doped region of the channel.

It has been demonstrated that graded-channel double gate MOSFETs can provide an intrinsic gain of about 90 dB in a wide temperature range.

REFERENCES


Electrical Properties of a Boron Doped Amorphous Silicon Bolometer Operating at Low Temperatures

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Abstract. We fabricated and characterized a-Si-B:H bolometers to be used as infrared sensors operating at low temperature. After a short review of bolometer properties required for this type of application, a detailed description of the fabrication process, and the characterization techniques are reported. We obtained values for the temperature coefficient of the resistance (TCR) higher than those reported in the literature, for the 77K-300K range of temperatures. The trade off between TCR and the electrical resistance of this bolometer is discussed, and conveniently parameterized in order to completely optimize the detector.

I Introduction

Bolometers are the best choice for direct detection of long wavelength radiation, 200 µm - 3000 µm, for far infrared and sub-mm astronomy applications [1,2]. One of the key issues for achieving low-cost detectors is their monolithic integration and compatibility with a CMOS technology. For this purpose, the most widely used cooled detector approach is to implement microbolometers using previously micromachined structures on CMOS processed wafers, thus achieving the required thermal isolation, as well as the feasibility to integrate them with other semiconductor devices. Currently at INAOE, we are developing bolometers based on boron doped hydrogenated amorphous silicon (a-Si-B:H) thin films. This particular material presents a high activation energy, which can be controlled easily by varying the doping level [3]. In addition to the high activation energy, the fabrication of these films is fully compatible with our CMOS technology, then we will be able to integrate the bolometer with the read-out circuitry; this will lead to bolometers with an improved performance when compared to those made of other different materials [4]. Since, our bolometer is intended for the detection of long wavelength infrared radiation, it will operate at low temperatures. The thermal isolation is achieved by depositing the a-Si-B:H thin film on a silicon nitride diaphragm, which is suspended on a micromachined crystalline silicon frame [5]. In this contribution we present the behavior of the most important electrical parameters of the bolometer: the electrical resistance R, and the temperature coefficient of resistance, measured in the 77K-300 K temperature range.

II Bolometer operation

A typical bolometer is normally formed by a temperature dependent resistor and an IR absorber; the same piece of material very often performs both functions. The
bolometer has a thermal capacity $C$, which is connected to a heat sink, or temperature reference $T_0$, through a link presenting certain thermal conductance $G$; this array is illustrated in Fig. 1.

![Diagram of a bolometer](image)

**Figure 1: Components of a typical a bolometer.**

The absorbed IR energy, $E$, increases the temperature of the bolometer to a value $T$. In order to maximize the temperature increase, $\Delta T = T - T_0 = E/C$, thus the sensibility, the bolometer must be thermally insulated (low $G$ values are needed), and must operate at low temperatures (low value of $C$). Recently, the use of micromachining techniques have allowed for obtaining a reduced thermal conductance. The electrical response depends on the temperature coefficient of resistance, TCR or $\alpha$, of the active element; this quantity is defined by [6]:

$$\alpha = \frac{1}{R_0} \frac{dR}{dT} \quad (1)$$

Thus, if the absorbed radiation rises the temperature of the element by an amount $\Delta T$, the electrical resistance increases by the amount

$$\Delta R = \alpha R_0 \Delta T \quad (2)$$

Where $R_0$ is the resistance at temperature $T_0$.

**III Thermal Analysis**

The heat flow diagram in Fig. 2 shows the related processes and the physical parameters that govern the thermal equilibrium of the bolometer for temperatures above the temperature $T_0$ of the heat sink. $P_r$ is the background radiation power; $P_j = I^2 R = V I$ is the Joule heat due to the bias current. The rate at which the heat is transferred from the bolometer to the heat sink is determined by the conductance $G(T)$. 

It is assumed that the system is under equilibrium condition when there is not any source of heat, but the background radiation (BGR). Therefore, the absorption due to the BGR causes a temperature change in the system until the thermal equilibrium is reached. The absorbed heat is then conducted to the heat sink through the link G(T). If k(T) is the thermal conductivity of the link at a temperature T, and considering the thermal resistance of a plate with a rectangular cross section of width W, length L, and thickness D, we have [7]:

\[ R_{th} = \frac{L}{kWD} \]  

In our device this plate corresponds to the silicon nitride diaphragm, with the following dimensions: W=203\,\mu m, L=300\,\mu m and D=0.15\,\mu m. According to figure 2, it is observed that total heat consist of two parts, the BGR (Pr) and the applied radiation Q. Let us consider the case Q=0; the optimal operation of the bolometer will depend on the contribution of both the BGR, Pr (coming from any surface at a temperature above the bolometer operating temperature, which can be due to a poor shielding against background radiation, chamber inner walls, etc.) and the power dissipated or Joule effect, PJ. The heat (power) will be conducted to the heat sink through G, giving rise to a local increment of temperature:

\[ G(T - T_0) = P_J + P_r \]  

If Pr is larger than PJ, it is possible to define a temperature T' for which:

\[ G(T' - T_0) = P_r \]

\[ G(T - T_0) = P_J \]  

The above equations show two limiting cases for the operation of a bolometer. The first one defines the operation limited by BGR, while the second marks the operation limited by the Joule effect or self-heating. Both limit the device’s performance; however, these effects can be reduced to a minimum making G small enough. Assuming that G is independent of T, i.e., it is only determined by the ambient/sink temperature T0, we can obtain equivalent voltage/current values:
\[ V(T) = \left[ R G(T - T_s) \right]^{1/2} \]  
\[ I(T) = \left[ R^{-1} G(T - T_s) \right]^{1/2} \]

By means of this set of equations, the values of \( G \) will be evaluated from the experimental measurements of the fabricated devices.

IV Deposition conditions for the sensor film

An AMP 3300 PECVD system from Applied Materials was used for the deposition of the amorphous films. The growth temperature was set to 270°C. The PECVD system is a planar reactor with a plate separation of 5 cm and 65 cm diameter. The RF power is supplied to the cathode (top electrode) through a matching network, and operates in the frequency range 8 to 111 kHz. A 100% SiH₄ and 1% B₂H₆/H₂ mixture was used as the gas source. In all the cases the pressure was maintained at 0.6 Torr, the RF power density was 0.09 W/cm² and the frequency was set to 110 KHz. The deposition time was 35 min, and resulted in film thicknesses in the 250 - 300 nm range. In order to obtain different boron content in the films, the flow ratio \( X_g = f_{B}H_6/(SiH_4 + B_2H_6) \), was varied.

V. Electrical characterization of the sensor films

Aluminum electrodes were deposited and patterned on the films. These structures were used to measure the current-voltage characteristics, which are shown in Figure 3 for different \( X_g \) values. A fairly ohmic behavior is clearly seen for all the samples; it can also be seen that the resistance of the samples varies with the content of boron. It is important to point out that it was not necessary a thermal treatment for alloying the Al to the B-doped a-Si:H film in order to obtain an ohmic contact. This is of fundamental importance since any thermal treatment at temperatures as low as 250°C can induce microcrystallization in the film, thus altering the electrical and optical properties of the sample [8].

![Fig. 3: I-V characteristics for the a-Si-B:H films for different boron content, \( X_g \).](image)

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The charge transport in amorphous materials (a-Si:H), is a thermally activated process, and the resistance can be expressed as \[ R(T) = R_0 \exp \left( \frac{E_a}{kT} \right) \] (8)

Where \( E_a \) is the activation energy, \( k \) is Boltzman’s constant, and \( T \) is the temperature. Using equation (8), and measuring the resistance of the films as a function of temperature, the activation energy may be estimated. Table I summarizes the obtained activation energies for the deposited films.

<table>
<thead>
<tr>
<th>( X_g )</th>
<th>( E_a ) (eV)</th>
<th>( \sigma ) (T=300 K), (( \Omega \cdot \text{cm})^{-1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.75</td>
<td>1.55x10^{-3}</td>
</tr>
<tr>
<td>0.06</td>
<td>0.48</td>
<td>4.05x10^{-3}</td>
</tr>
<tr>
<td>0.091</td>
<td>0.43</td>
<td>1.21x10^{-4}</td>
</tr>
<tr>
<td>0.12</td>
<td>0.46</td>
<td>8.77x10^{-5}</td>
</tr>
</tbody>
</table>

Using equations (8) and (1), the TCR can be written as

\[ \alpha = -\frac{E_a}{kT^2} \] (9)

It is clear from equation (9) that a high sensitivity corresponds to a high activation energy. It is worth mentioning that the activation energy depends on the doping [1], since the activation energy becomes higher for lower doping concentration. On the other hand, a high activation energy leads to a high resistivity, which is undesirable for the read-out electronics connected to the bolometer; thus the circuitry sets an upper limit to the bolometer electrical resistance. Consequently, a trade off must be found between the TCR and the bolometer resistance.
Fig. 4: Activation energy ($E_a$) and dark conductivity ($\sigma$) of the B-doped a-Si: H films with a varying boron content

As is depicted in figure 4, for the depositing conditions used in this work and for the RF frequency set at 110kHz, there is a continuous increase in the dark conductivity of the deposited films for an increasing $X_g$. This behavior is observed until $X_g = 0.091$. After that point, the dark conductivity starts to decrease. It is observed an increase in the conductivity up to 4 orders of magnitude with respect to the un-doped material. When $X_g > 0.091$, $\sigma$ starts to decrease. An opposite trend is observed for the activation energy. In this case the minimum value is obtained for the corresponding point of maximum dark conductivity.

VI Bolometer Fabrication

The thermal isolation was obtained by depositing the sensing film on a thermally and electrically insulating silicon nitride membrane sustained by a micromachined c-Si frame [2,3,4]. The final structure is shown in Fig. 5. The 150 nm-thick silicon nitride film was deposited by LPCVD. The c-Si wafer was micro machined using a KOH solution at 80°C for 5 hours. An AMP 3300 PECVD system from Applied Materials was used to deposit the amorphous silicon films, with the best properties ($X_g = 0.091$); the substrate was kept at 270 °C. This 170 nm-thick a-Si film was deposited at 0.6 Torr by decomposing a SiH₄–B₂H₆ mixture with a 750-scc/min flux. The deposition rate was 1.3 Å/s for an RF power of 300 W and 110 KHz [5]. Finally, aluminum was deposited and patterned to form contact pads.
Figure 5: (a) Cross section view, and (b) top view of the bolometer structure. The sensor layer has an area of 37x37 μm².

VII Room Temperature Characterization of the bolometer

The resistance of the devices was measured using an HP Semiconductor Parameter Analyzer, under vacuum (7 mTorr), and the voltage was swept between -10V and 10V, under dark conditions. Typical results are shown in Fig. 6.

Figure 6: Measured current-voltage characteristics of the bolometers at room temperature.
The electrical resistance, $R$, is the inverse of the slope obtained from the measured I-V curve, and can be expressed as [10]

$$R = \frac{\rho}{kd}$$

(10)

Where $k$ is a geometrical correction factor, $\rho$ is the resistivity, and $d$ is the thickness of the sample (0.17 $\mu$m). A conformal transformation was employed to determine this geometrical factor, and a value of $k=0.472$ is obtained from [10].

According to Fig.6, a fairly ohmic behavior is clearly seen, and the slope of the I-V curve is almost constant, showing that efficient contacts were obtained. The bolometer performance is limited by both the BGR and Joule effect. The BGR impact on the device, as a function of time, is shown in Figure 7.

![Figure 7: Change of the resistance due to the background radiation as a function of time.](image)

**VIII Measurements at Low Temperatures**

After measuring the room temperature characteristics of the bolometers, their characteristics were measured in the temperature range 77K-300K. An open cycle cryostat was used in this experiment, with LN2 as the cryogen. The samples were silver epoxied at the copper plate of a 24-pins, dual in line, ceramic package, and contacted with 50 $\mu$m diameter bonded aluminum wires; the encapsulated device can be seen in Figure 7.
Inside the vacuum chamber, the package was mounted on a copper holder placed in the cold finger. The temperature was measured using a calibrated Lake Shore Si diode thermometer. The experimental R-T measured values in the above mentioned range are shown in Figure 9.

From the measured resistance, the TCR can be estimated using equations (8) and (9). Figure 10 shows the obtained TCR values, which varies from -0.034 at 300K to -0.2 at 77K, showing an increase of 6 times.
At 77 K, the bolometers showed to be very sensitive for small amounts of absorbed energy that is radiated by the inner walls of the vacuum chamber. For instance, the temperature fluctuations of the external walls, which are exposed to the ambient, produced small variations in the temperature of the inner walls; this led to a fluctuating radiation being absorbed by the bolometer (the radiation shield was removed in this experiment). This effect can be seen as a change in the I-V curves, as shown in Figure 11. A slight variation of the bolometer temperature (ΔT ~ 0.02K) produced a resistance variation of 255.009 kΩ at 77 K, while at room temperature the same ΔT resulted in a resistance change of 1.89 MΩ. These results agree with a very high TCR.

Figure 10: TCR as a function of the temperature.

Figure 11: Response of I-V curves due to the room temperature change from 293.2 to 296.5 K at 77K.

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From these changes in resistance, considering the $\text{TCR} = 1/R^*\Delta R/\Delta T$, and using equations (6) and (7), we can now calculate the thermal conductance. The calculated thermal conductance at room temperature is $1.8 \times 10^{-6}$ W/K, which is similar to that reported in the literature [11]. From these calculated value and using equation (3) we estimate a thermal conductivity of $\kappa = 0.158 \text{ W/cm-K}$.

In order to be assure that those fluctuations were due to the external variations of temperature and that the film was stable, a radiation shield was placed on the top of the packaged bolometer inside the cryostat. No change in the I-V characteristics was observed for different periods of time. This is shown in figure 12.

![Graph](image)

**Figure 12: Behavior I-V of bolometer to dark and closed to different time.**

**IX Conclusions**

A very sensitive bolometer using boron doped amorphous silicon thin films was presented. Our device showed a higher TCR than those previously reported for a-Si:H, and electrical resistances in the order of $\text{M}$, which are suitable for matching the read-out circuitry for a monolithic integration of the bolometer. The obtained TCR values ranges from $-0.034$ at 300K to $-0.2$ at 77K. Therefore, this material and its fabrication is an excellent candidate for IR imaging at long wavelengths.

**X Acknowledgments**

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XI References


CRYOGENIC OPERATION OF HIGH-VOLTAGE IGBTs

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ABSTRACT

The size, weight, and losses of high-voltage power systems for space-based and other applications can be reduced by utilizing cryogenically cooled IGBTs. This paper presents experimental data and test results of devices cryogenically rated at 1.3- to 5.0-kV, including such key parameters as on-state voltage, switching times, and switching energies for the temperature range between 77 K and 400 K. The measurement results are discussed.

INTRODUCTION

Cryogenic Power Electronics

The largest and heaviest components in any power electronics system are often the filter inductors and capacitors. These can be made smaller and lighter by operating the system at higher frequencies. However, this operating frequency is limited by the speed of the switching device used. While MOSFETs are extremely fast, and can operate at very high switching frequencies, they are only good up to about 1 kV. For higher voltages, the next-best device is the Insulated Gate Bipolar Transistor (IGBT). IGBTs are, however, much slower than MOSFETs, and therefore are not capable of the same range of operating frequency.

By cryogenically cooling IGBTs, considerable gains in switching speed can be obtained, making these devices possible candidates for small, light-weight, high-frequency power systems. The reason for this increase in the switching speed is the decrease in carrier lifetime at low temperatures. IGBTs are minority carrier devices whose transition times are determined by how quickly the device can store and release charges. Charge storage, in turn, is a function of carrier lifetime, which decreases at low temperatures, leading to faster transition times.

In addition to this increase in switching speed, cryogenic IGBTs also exhibit lower on-state voltages, and, with that, lower conduction losses. These improvements are not as great as in MOSFETs at low temperatures, but could nonetheless prove useful in certain applications.
Devices Tested and Measurement Techniques

Eight medium-high and very-high voltage devices of varying current capabilities and device structures were studied. The medium-high-voltage devices were rated in the 1.3- to 1.7-kV range at cryogenic temperatures with rated currents of 15, 20, 50, and 60 A. The high-voltage devices were rated at 2.5 and 5.0 kV and at currents of 50 and 200 A. Test circuits were constructed to measure on-state voltage, switching speed, and switching energies at various temperatures.

TEST RESULTS

Medium-High-Voltage IGBTs

**MIG-01 IGBT (1.3 kV, 15 A).** The on-state voltages of a 1.3-kV, 15-A IGBT at 77 K (-196 °C) and 400 K (+125 °C), for 100 μs pulses, are shown in Figure 1. These measurements illustrate the drastically improved current handling capability at low temperatures, more than 100 A for the device rated 15 A (at 80 °C). The device also exhibited large improvements in switching speed. Figure 2 shows the switching curves at 400 K, 300 K and 77 K with a load resistor of 100 Ω at 1.24 kV (12 A). The voltage rise-time during turn-off dropped from 282 ns at 400 K to 33 ns at 77 K, and was 8.5 times faster. This improvement approaches the cooling penalty, or the energy expended to cool the device, especially in space applications, and therefore helps to compensate for it. The turn-on time was even lower, only 16 ns.

**MIG-02 IGBT (1.3 kV, 50 A).** The resistive turn-off current rise and voltage fall times of a 1.3-kV, 50-A device were measured as a function of temperature at 1200 V, 60 A. Due to the so-called tail current and lead inductances, the turn-off current fall time is larger than the voltage turn-off rise time. Figures 3 and 4 show the waveforms at 400 K and 77 K. Trace M is the product of the voltage and current (channels 1 and 2), and represents the turn-off power. Note the long tail current of more than one microsecond duration at high temperature, whereas at 77 K the turn-off is basically finished in 100 ns. The voltage rise time during turn-off is 299 ns at 135 °C and 43.3 ns at 77 K. The improvement factor is 6.9. One can also see that the high speed at low temperature requires a better RF circuit layout. Nevertheless, one can summarize that this device works very well down to the temperature of liquid nitrogen with reduced conduction and switching losses that compensate for the cooling penalty. The rise and fall times are shown as function of temperature in Figure 5.

The breakdown voltage of this 1700 V transistor was also measured at 77 K, and was found to decrease to 1380 V. This corresponds to a reduction of 19%, about the same measured for power MOSFETs.

**MIG-06 IGBT (1.3 kV, 60 A).** The 1.3-kV, 60-A device had a different IGBT chip structure than did the MIG-01 and MIG-02, and this device was observed to "freeze out" at about -100 °C, meaning that the device does not reach full conduction at low temperatures. This effect is marked by a sharp rise in on-state voltage, and therefore in the on-state resistance of the device. The freeze-out is attributed to an additional n+ layer in front of the collector p-region that is not found in most other device structures. It is
also noteworthy that the temperature coefficient of the on-state voltage is much smaller than in the previously described IGBTs, and thus very little change in on-state resistance was measured before the device froze out.

Even more interesting is the switching behavior of this device, which exhibits a very large (20 A at 200 ns) and also very long (>1 μs) tail current at 425 K. This tail current disappears almost completely at 77 K, translating into a drastic reduction in the turn-off losses through cryo-cooling. However, the 77-K on-state voltage is about 250 V at this operating current because of the freeze-out effect. Nevertheless, the device can carry 60 A, even in this condition. For longer or repetitive current pulses, internal junction heating will reduce the on-state voltage. This can be seen in Figure 6, where a 50-μs pulse is displayed with the device immersed in liquid nitrogen (LN₂). After about 30 μs the on-state voltage is reduced to its low level. This sharp change in on-state voltage can be used to determine the thermal impedance of the device at cryogenic temperatures. Figure 7 plots the switching times as functions of temperature. Compared with the 425 K turn-off, the improvement factors are 5.6 and 24 for the current and voltage switching times, respectively!

**MIG-08, MIG-09 IGBTs (1.7 kV, 20 A).** A factor of 22 decrease was measured in the turn-off voltage rise times of 1.7-kV, 20-A IGBTs, part numbers MIG-08 and MIG-09. A 6.8 times improvement was also observed in the turn-on voltage fall times. The pulse width was 100 μs. In Figures 8 and 9, the switching turn-on and turn-off powers and energies are presented as functions of time and temperature. The measured transition times are plotted as functions of temperature in Figure 10. The total switching losses of this device are reduced by about a factor of 6 through cryo-cooling, which should approach or exceed the cooling penalty in the extreme environments of space travel.

**Very High-Voltage IGBTs**

**MIG-07 IGBT (2.5 kV, 50 A).** Figure 11 shows the current and voltage curves of a 2.5-kV, 50-A IGBT. Again there is a considerable reduction in on-state voltage at high currents achieved by cryo-cooling the device to 77 K. At 100 A, the loss-producing on-state voltage is reduced by about 2 V. The turn-off waveforms and switching times did not change much between 300 K and 77 K. Tables 1 and 2 summarize the results. While this device did not exhibit the expected drastic reduction in turn-off times and losses, it did operate at 77 K. This may be important for certain applications.

<table>
<thead>
<tr>
<th>Temperature (Kelvin) (1800 V)</th>
<th>Current Rise Time (Turn-On)</th>
<th>Current Fall Time (Turn-Off)</th>
<th>Voltage Fall Time (Turn-On)</th>
<th>Voltage Rise Time (Turn-Off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 K</td>
<td>126 ns</td>
<td>570 ns</td>
<td>19.0 ns</td>
<td>466 ns</td>
</tr>
<tr>
<td>77 K</td>
<td>95.6 ns</td>
<td>706 ns</td>
<td>9.24 ns</td>
<td>395 ns</td>
</tr>
</tbody>
</table>

Table 1: Comparison of switching speeds at various temperatures. The input voltage was 1800 V, the load resistance was 50 Ω and the pulse width was 10 μs.
### Table 2: Comparison of switching energies at various temperatures. The input voltage was 1400 V, the load resistance 50 Ω, and the pulse width 116 µs.

<table>
<thead>
<tr>
<th>Temperature (Kelvin)</th>
<th>Turn-On Energy (J)</th>
<th>Turn-Off Energy (J)</th>
</tr>
</thead>
<tbody>
<tr>
<td>420 K</td>
<td>1.02</td>
<td>12.0</td>
</tr>
<tr>
<td>300 K</td>
<td>0.27</td>
<td>10.6</td>
</tr>
<tr>
<td>77 K</td>
<td>0.08</td>
<td>7.8</td>
</tr>
<tr>
<td>Improvement Factor</td>
<td>12.75</td>
<td>1.54</td>
</tr>
</tbody>
</table>

MIG-03 IGBT (2.5 kV, 200 A). Figure 12 shows the measured on-state voltage (V_{ce}) of a different 2.5-kV IGBT (rated at 200 A) at 400 K and 77 K. At high currents V_{CE} drops by more than a factor of two at low temperatures, a good improvement. But the most remarkable feature is that the current handling capability of the 200-A rated device is over 1000 A at 77 K. This again demonstrates the tremendous overload potential of cryo-cooled IGBTs and other semiconductor devices. Another interesting feature is that at V_{CE} = 3 V, the current is about 3 times higher at 77 K than at 400 K. No freeze-out was observed down to 77 K.

The device’s voltage and current rise and fall times for a 500-kVA pulse (2000 V, 250 A, R_{load} = 8 Ω) were 477 ns and 494 ns, and 358 ns and 342 ns, respectively. At higher temperatures, up to about 140 °C, the switching times remain more or less constant. They also stayed roughly constant down to about −150 °C before increasing. Although the device works fine at 77 K, it does not exhibit the hoped-for increase in switching speeds that was observed in the medium-high-voltage IGBTs. In fact, the switching times of this device actually increased to between 1.2µs and 1.3 µs at 77 K. We do not yet understand this behavior. There may be considerable differences in the device structures of low voltage (up to 1700 V) IGBTs and HV (2.5 kV to 5 kV) IGBTs.

MIG-04 IGBT (5.0 kV, 50 A). The on-state voltage curves of a 5-kV, 50-A IGBT are shown in Figure 13. At a collector-emitter voltage of 5 V, the current at 128 °C is 20 A, but the current increases five times to 100 A at −100 °C! At 50 A, V_{CE} drops from 8 V to 3.5 V over this temperature range, improving by a factor of 2.28. However, this device also went into the freeze-out mode, this time at −140°C. The MIG-04 also contains a thin n+ layer inserted by ion implantation before the p+ collector, and is similar in structure to the MIG-06 (which froze out at −100 °C). The switching times showed no significant change down to −100 °C.

MIG-10 IGBT (5.0 kV, 200 A). Also tested was a 5-kV, 200-A IGBT module. This device, however, did not exhibit a freeze-out down to 77 K, as shown by the I-V curves of Figure 14. In fact, the device was able to pass currents of over 1000 A at low temperatures. Nevertheless, the switching times behaved similarly to those of the MIG-04, and showed no considerable change down to 77 K.
CONCLUSIONS

A wide variety of device structures and manufacturing technologies are used to produce different IGBTs, and this study demonstrates that the temperature-dependent behavior of these structures varies from type to type. This makes it difficult to generalize the suitability of IGBTs for Cryo-Power applications. The main problem with all these devices is that the diode voltage drop determines the on-state voltage threshold, and thereby limits the improvement factors achievable through cryo-cooling. It has been difficult to identify the causes of improvements in the temperature dependence because of the reluctance of manufacturers to disclose details of their products, including such issues as radiation for lifetime treatment and doping concentrations, which could seriously affect a device's performance at low temperatures. Nevertheless, vast improvements were observed in switching speeds of some select devices with low-temperature ratings of up to 2.5 kV, even in those devices that froze out at temperatures above 77 K. The 1.3- to 2.5-kV devices studied also showed vast improvements in on-state voltage. The 5-kV devices reported here did not improve much in either respect.

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Figure 1: I-V on-state curves for a MIG-01 IGBT (1300-V, 15-A) at 400 K, 300 K, and 77 K.

Figure 2: Turn-off switching times of the MIG-01 IGBT (1300 V, 15 A), showing a factor of 8.5 improvement at 77 K compared to 400 K.
Figure 3: 135°C (408 K) turn-off waveforms for the MIG-02 IGBT (1300 V, 50 A). The uppermost curve illustrates the energy losses during the turn-off transition. Note the tail current after the dashed line. (Ch. 1: 1 V = 100 A)

Figure 4: 77-K turn-off waveforms of the MIG-02 IGBT (1300 V, 50 A). Note the reduction of the tail current compared to Figure 4, and the reduction in voltage rise time from 299 ns at 135°C to 4.3 ns at -196°C (a factor of 6.9). (Ch. 1: 1 V = 100 A).
Figure 5: Turn-off switching times of the MIG-02 IGBT (1300 V, 50 A) showing a factor of 4 to 6 decrease between +140 °C (413 K) and -196 °C (77 K).

Figure 6: 50-μs pulse of the MIG-06 IGBT (1300 V, 60 A) at 77 K (−196 °C). Note the reduction of on-state voltage during the pulse due to elimination of carrier freeze-out through junction heating.
MIG-08: 1.7 kV, 20 A IGBT

Figure 7: Turn-off switching times (current fall time and voltage rise time) of the MIG-06 IGBT (1300 V, 60 A) as functions of temperature.

MIG-08: 1.7 kV, 20 A IGBT

Figure 8: Smoothed turn-on energies for the MIG-08 (1700 V, 20 A) at various temperatures, showing a 26 times improvement at 77 K compared to 400 K.
Figure 9: Turn-off energies for the MIG-08 (1700 V, 20 A) IGBT at various temperatures, showing a 7 times improvement between 400 K and 77 K.

Figure 10: Transition times for a MIG-08 IGBT (1700 V, 20 A) as functions of temperature.
Figure 11: Current-voltage characteristic curves of the MIG-07 IGBT (2.5 kV). The 50-A line corresponds to the 200-A line of a module made with four of these chips.

Figure 12: Current as a function of on-state voltage for the MIG-03 IGBT Module (2.5-kV, 200-A), showing a significant improvement at 77 K (-196 °C) over 400-K (125 °C) operation. Note the 1000-A pulse capability at 77 K.
Figure 13: I-V characteristics of a MIG-04 IGBT (5-kV, 50-A) at various temperatures.

Figure 14: Current-voltage characteristic curves of the MIG-10 IGBT module (5 kV, 200 A) at 400, 300 and 77 K, showing that much higher currents can be reached at lower temperatures.
Ge SEMICONDUCTOR DEVICES FOR CRYOGENIC POWER ELECTRONICS - IV


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ABSTRACT

We have been developing semiconductor devices (diodes and transistors), based on germanium, for cryogenic power applications. Target applications include spacecraft for cold environments as well as commercial, industrial, and defense systems that incorporate cryogenics. The applications and motivation for this work are presented elsewhere [1-3].

Our primary reason for basing these devices on Ge is that it enables good performance down to deep cryogenic temperatures (down to 20 K and lower), although there are other advantages to using Ge such as a low p-n junction forward voltage and high mobility.

During this development we have designed, fabricated and characterized the following devices:

(1) Ge power diodes (10 A) that operate from room temperature to approximately 20 K. Their forward voltage is about half that of Si power diodes and we have achieved reverse breakdown voltage as high as 400 V from room temperature down to 20 K

(2) Ge JFETs with an Idsat of more than 0.5 A at liquid-nitrogen and liquid-helium temperatures, and a transconductance of approximately 200-300 mS at cryogenic temperatures.

(3) Ge MISFETs with 10 W capability that operate from room temperature to liquid-helium temperature (Figure 1). Transconductance is approximately 100 mS for all temperatures.

We thus believe that Ge power devices are practical and offer important advantages for cryogenic space and ground applications.
Figure 1: Output characteristics of Ge n-channel enhancement MOSFET in liquid helium. Vert = 0.1 A/div, hor = 2 V/div, $\Delta V_{gs} = 1$ V step.


ANALOG POWER AND DIGITAL CIRCUITS AT CRYOGENIC TEMPERATURES FOR SPACE

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ABSTRACT

This paper reports on the design, fabrication and testing of wide bandgap engineered digital circuits (Inverter and NAND gate) and analog power devices using metal-oxide-semiconductor modulation-doped-field-effect-transistors (MOS-MODFETs) for space-borne cryogenic applications using silicon-germanium technology.

Analog and digital devices capable of low temperature operation are invaluable aboard space probes. On earth, or near the sun in general, radiation from the sun keeps electronic circuits warm. As space probes move farther from the sun however, they experience low temperatures. For example, the temperature on the Martian surface varies from only 10 °C on a summer day down to about -115 °C on a winter night. And it gets worse further away from the sun: near Pluto’s orbit, temperatures can reach about 40 K (-233 °C). Ordinary silicon based electronic devices and circuits fail at these cryogenic temperatures. To get around this problem, space research organizations such as NASA currently place electronic circuits in a warm electronics box (WEB) that is kept heated by radio-isotope heating units (RHUs) containing plutonium-238. Although these RHUs do solve the problem of low temperatures affecting device performance, they also have disadvantages. They add to the weight of the spacecraft, have constant and uncontrollable heat output, and pose an environmental threat in case of a failed launch or during re-entry of the spacecraft into the earth’s atmosphere. Electronic devices and circuits capable of operation at cryogenic temperatures may offer a much better solution.

Highly doped silicon, germanium or silicon-germanium does not freeze out even at low temperatures. Although highly doped semiconductors are usually of no use in bulk device (except for making ohmic contacts), the property of highly doped semiconductors may be exploited to obtain modulation-doped heterostructures that exhibit high mobility even at low temperatures. If a heterojunction is made between two materials for which there exists a continuum of solid solutions, such as between Si and Ge (Si$_{1-x}$Ge$_x$ exists for all x such that 0<x<1), the chemical transition need not occur abruptly. Instead, the heterojunction may be “graded” over some specified distance. That is, the composition parameter x might be some continuous function of the position. Such heterojunctions have desirable properties for cryogenic applications in deep space. Modulation doping in a semiconductor heterostructure allows high carrier mobilities to be attained at lower temperatures.
A modulation-doped heterostructure allows charge carriers to remain highly mobile even at low temperatures by implementing the following two conditions, which must be satisfied under all possible operating conditions.

The charge carriers must be placed in a channel region, separated from the ionized dopants. The source of the carriers, i.e. the supply layer, must be highly doped in order to prevent carrier freeze-out at low temperatures. The first condition is necessary to minimize ionized-impurity scattering. The second is necessary because highly doped (>10^17 approximately) Si, Ge or SiGe does not freeze out. Layer design usually starts with selecting the compositions of the active layers and of the virtual substrates, which define the band offsets.

One-dimensional Poisson solvers were used to obtain the band structure of the silicon-germanium heterostructure and electron densities in the conducting channel. The structure chosen for growth was 38-63 ohm-cm boron doped P-type silicon substrate. The first layer is a graded SiGe buffer in which the Ge concentration is increased from 0 to 30%. Next is a 1 micrometer thick relaxed Si$_{0.7}$Ge$_{0.3}$ layer. Together these layers form the virtual substrate on which a strained Si layer may be grown. This is followed by a 5 nm thick Si$_{0.7}$Ge$_{0.3}$ supply layer doped with Sb to 5x10^18/cm^3. The 3 nm thick undoped Si$_{0.7}$Ge$_{0.3}$ layer is a spacer and prevents electrons in the following 8nm undoped strained Si channel from interacting with the ionized impurities in the supply layer. The channel is followed by a 5 nm thick undoped Si$_{0.7}$Ge$_{0.3}$ barrier layer which prevents electrons from the supply layer from accumulating in the cap. The cap itself is a 10 nm thick undoped Si layer which was almost completely consumed during thermal gate oxidation. The results show that the electrons are confined to the channel region, and not present in the cap in high concentrations. Changing the amount of applied gate bias produced a change in the electron density in the channel which indicated the ability of the gate to modulate drain-source current.

The finished device was mounted on a 24-pin DIP package with conductive adhesive. The pads on the device were bonded to the package pins with 25 micrometer gold wire. The packaged device was mounted on the cold head of a CTI-Cryogenics Model 22 helium refrigerator. A HP 4145B semiconductor parameter analyzer was used to obtain current-voltage characteristics. The drain source breakdown voltages were greater than 30 V. The gate leakage current at VGS = 10 V was found to be less than 1 nA. The gate to body capacitance CGB was found to be 1.4 pF. The devices were tested in a simple class-A amplifier circuit, where they produced a power output of 9 mA p-p at 3 V for an input of 3 V, 1 microampere p-p, indicating significant power gain. The current-voltage characteristics as well as transfer characteristics of the devices demonstrated the feasibility of using n-channel and p-channel MODFET's for power devices as well as for digital circuits from 300 K to 40 K.

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SiGe SEMICONDUCTOR DEVICES FOR CRYOGENIC POWER ELECTRONICS

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ABSTRACT

We are taking the initial steps in developing power semiconductor devices based on the silicon-germanium (SiGe) materials system. The applications and motivation are similar to those for our development of Ge devices described elsewhere [1], namely spacecraft for cold environments as well as commercial, industrial, and defense systems that incorporate cryogenics.

The SiGe materials system has proved its benefits in devices for telecommunications. It also has valuable features for power electronics and cryogenic operation. Our objective is to take advantage of the features of SiGe in combination with those of Si and Ge to develop diodes and transistors for cryogenic power operation. These features include:

- **Si**: an extensive technology base, high breakdown voltage, an excellent grown oxide.
- **Ge**: low p-n junction forward voltage, low freeze-out temperature, high mobility at low temperature.
- **SiGe**: bandgap engineering, selective placement, a developing technology base and compatibility with Si processing.

The first device that we are working to develop for cryogenic power is the hetero-junction bipolar transistor (HBT). These follow a standard design, using SiGe for the base region to maintain high gain over a wide temperature range from room temperature to deep cryogenic temperatures. However, we are designing the structure for high current and voltage.

Initial results are encouraging, although falling short of our goal. Figure 1 is an example of the characteristics of one of our devices in liquid nitrogen. It exhibits adequate current and voltage capability for a prototype, but its current gain is only slightly larger than 1. However, the current gain increases upon cooling from room to liquid-nitrogen temperature, which is an important outcome.
The charge carriers must be placed in a channel region, separated from the ionized dopants. The source of the carriers, i.e. the supply layer, must be highly doped in order to prevent carrier freeze-out at low temperatures. The first condition is necessary to minimize ionized-impurity scattering. The second is necessary because highly doped (>10^{17} approximately) Si, Ge or SiGe does not freeze out. Layer design usually starts with selecting the compositions of the active layers and of the virtual substrates, which define the band offsets.

![Bipolar characteristics at liquid-nitrogen temperature](image)

**Figure 1:** Bipolar characteristics at liquid-nitrogen temperature, the looping and "droop" at high current and voltage are evidence of heating at high power (~10 W). Vert = 20 mA/div, horiz = 5 V/div, ΔI_b = 20 mA/step.

Using more appropriate materials and designs we expect to improve the characteristics considerably.

In conjunction with the HBT work we are also developing MIS structures. Successful development of bipolar and MIS structures could then form the basis for fabrication of more complex power devices for cryogenic operation, such as the *insulated-gate bipolar transistor* (IGBT) and *MOS-controlled thyristor* (MCT).


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LIQUID HELIUM TEMPERATURE IRRADIATION EFFECTS ON THE OPERATION OF 0.7 μm CMOS DEVICES FOR CRYOGENIC SPACE APPLICATIONS

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ABSTRACT

This paper describes the impact of ionising irradiation, performed at liquid helium temperatures (LHT) on the characteristics of transistors that have been fabricated in a 0.7 μm CMOS technology. First, a brief description of the cryogenic irradiation set-up and the pre- and post-irradiation characterisation will be given. Next, the behaviour of the input and output characteristics at LHT is described before and after γ-exposure to a total dose of 15 to 30 kr(Si), which is the expected total dose range for the Herschel mission, scheduled for launch in the spring of 2007. The observed changes in the static device parameters at LHT will be compared with earlier results, obtained after room temperature irradiations. Overall, it is concluded that the components are sufficiently radiation hard for the considered space mission, from a viewpoint of Total Ionisation Dose damage.

INTRODUCTION

The Herschel Space Observatory, an ESA cornerstone mission to be launched in spring 2007, will explore the formation and evolution of galaxies and stars through photometric and spectroscopic observations in the far-infrared and submillimeter wavelength range. The satellite will be equipped with a 3.5 m telescope, passively cooled to ~75 K, and a liquid Helium cryostat for the focal plane instruments, the Photodetector Array Camera & Spectrometer (PACS). PACS will be a combined imaging photo/spectrometer for the wavelength range 57–210 μm. The technology of choice for LHT circuitry used for PACS is clearly CMOS, as the current gain of bipolar transistors is normally very small at 4.2K. However, one should take into account the particular device behavior at these temperatures as they suffer from carrier freeze out and related transient and kink effects. All this indicates that the problem of radiation hardness of cryogenic electronics is a complex interplay between technology design and operation conditions. The difficulties associated with predicting the radiation response of cryogenic circuitry based on room temperature irradiation studies has already been pointed out on several occasions [1-4].

Thus, radiation testing should preferably be performed at operating temperatures, which is not always straightforward (e.g., practical problems related to operating devices at liquid helium temperatures). The basic reason for the temperature impact on the radiation response is that the created charge or damage in the dielectric...
layers is essentially frozen (immobile) at deep cryogenic temperatures, which eliminates some temperature driven processes like interface state formation [5-7] or emphasizes some specific degradation mechanisms at low temperature (T), like the lateral non-uniformity of the dose deposition [8-10] or enhanced Coulombic scattering at oxide-trapped charge [11]. As a result, it may be argued that Total Ionising Dose (TID) damage is expected to be worse at low temperatures compared with room temperature.

The aim of the paper is to report on the radiation response of transistors, fabricated in a 0.7 μm CMOS technology, used for prototyping the cryogenic read-out circuits (CRE's) [12] for the Herschel mission of the European Space Agency (ESA). Previously, similar components have been irradiated at room temperature, but tested at 4.2 K [13]. This produced marked changes in the input and output characteristics of the transistors [13-15], which also depended on technological details, like, e.g., the presence of a lowly-doped drain (LDD) or a p-well. An example is given in Figs 1 and 2, showing the input I_D (drain current) versus V_GS (gate voltage) and G_m (transconductance) versus V_GS characteristics, respectively, of a 10 μmx5 μm n-MOSFET at 4.2 K, before and after a 50 krd(Si) 60Co γ-irradiation, performed at room temperature. One can notice a clear increase of I_D and G_m and a reduction of the threshold voltage, which has been ascribed to the reduction of the series resistance, associated with the LDD regions, which are frozen-out at 4.2 K [13,14]. In addition, curves are represented in Figs 1 and 2, recorded after a few weeks of unbiased room temperature annealing and showing a partial recovery of the characteristics. This teaches us first of all that post-irradiation testing should be done immediately after the end of the irradiation to avoid possible annealing of the damage. This is even more so for cryogenic exposures, where one should avoid heating of the sample in between the irradiation and the testing. Secondly, since these γ-exposures typically take a few hours, one can expect some thermally activated annealing to occur, if performed at 300 K, which will be suppressed for an irradiation at LHT.

Fig. 1. Input characteristics of a 10 μmx5 μm LDD n-MOSFET in linear operation (drain bias V_Ds=0.025 V) and at T=4.2 K before and after a 50 krd(Si) γ-irradiation, performed at room temperature (RT). The dashed line corresponds to the curve obtained after a few weeks of room temperature unbiased annealing.
Fig. 2. Transconductance versus gate voltage of a 10 μm x 5 μm LDD n-MOSFET in linear operation (drain bias V_{DS}=0.025 V) and at T=4.2 K before and after a 50 krad(Si) γ-irradiation, performed at room temperature (RT). The dashed line corresponds to the curve obtained after a few weeks of room temperature unbiased annealing.

Therefore, a cryogenic irradiation facility has been assembled. This dedicated system for in situ irradiation and testing at low temperature (4-7 K) has been described in more detail in another contribution [16]. Here, mainly results will be reported on the impact of 60Co γ-irradiation on the in- and output characteristics of 0.7 μm CMOS n- and p-channel transistor. The implications on circuit operation will also be briefly addressed.

**EXPERIMENTAL**

The components studied were selected single devices of an amplifier used in the Photodetector Array Camera and Spectrometer (PACS) CRE circuit [12], which were mounted in a 40 pin dual-in-line package. The gate length of the transistors (L) was 10 μm; their width W=22 μm (n-) or 130/65 μm (p-MOSFET). For each amplifier 7 transistors were fully characterized: 4 p-MOSFET: M13, M12 (W/L= 65 μm/10 μm) and M4, M5 (W/L= 130 μm/10 μm) and 3 n-MOSFETs: M11, M20, M21 (W/L= 22 μm/10 μm). During the irradiation, a constant bias of +5 V was applied to the gates of the n-MOSFETs, while all the other terminals were grounded, including the gate of the p-MOSFETs. This should be the worst case biasing condition from a viewpoint of TID damage for bulk CMOS. The amplifier was fabricated in a standard, single poly 0.7 μm CMOS technology at AMI Semiconductor in Oudenaarde (Belgium).
The packages were mounted in a liquid helium flow cryostat from JANIS, which was evacuated and had a typical base temperature of 5 to 7 K. $^{60}$Co γ-irradiations were performed at a dose rate of $\sim$100 rd(Si)/min up to a total dose of 15 or 30 krd(Si), employing the ESTEC $^{60}$Co radiation facility. The predicted End-of-Life TID received by the Herschel spacecraft is 15 krd(Si). During the irradiations, the temperature remained stable and did not show a marked increase, due to the absorbed radiation power [16]. Part of the experimental arrangement is shown in Fig. 3. The steering electronics was outside the irradiation room and connected by feed-throughs in the wall of the chamber. This is schematically illustrated in Fig 4.

Fig. 3. Cryostat at the γ-source in ESTEC before the start of a cold γ-irradiation.

Fig. 4. Block diagram of the measurement set-up.
The input and output characteristics of the transistors were measured by an Agilent Parameter Analyzer, as indicated in Fig. 4.

RESULTS AND DISCUSSION

Pre and post 15 krd(Si) γ-irradiation results of an n- and a p-channel transistor are illustrated in Figs 5 and 6. It is observed in Fig. 5, that there is only a minor change in the threshold voltage (<90 mV) or the maximum transconductance (Figs 5a and 6a). Notice also the negligible kink effect in saturation (Fig. 5b) for these n-type devices, which demonstrates their suitability for cryogenic space operation. The same conclusion can be drawn for the p-channel transistors, based on the results of Fig. 6. Thus, it is concluded that at the transistor level this 0.7 μm CMOS technology is sufficiently hard to survive the expected TID during the Herschel mission.

Fig. 5. Input (a) and output (b) characteristics of a 22 μm by 10 μm n-MOSFET at 7 K, before and after a 15 krd(Si) γ-irradiation. The drain voltage is 25 mV (a) and the gate voltage is changed from 1 to 5 V, with a step of 1 V (b)
Fig. 6. Input (a) and output (b) characteristics of a 130 µm by 10 µm p-MOSFET at 7 K, before and after a 15 krd(Si) γ-irradiation. The drain voltage is -25 mV (a) and the gate voltage is changed from -1 to -5 V, with a step of -1 V (b).

Compared with the previous results, obtained after a room temperature exposure, the following can be noticed. For the n-channel transistors, a reduction of $I_D$ and $G_m$ is found after a LHT γ-irradiation, which is opposite to the trends observed in Figs 1 and 2. This can most likely be explained by the fact that the transistors studied here did not have an LDD. Moreover, exposure at LHT predominantly leads to radiation-induced hole trapping in the oxide and no creation of interface traps [5-7,17]. This implies that for an n-channel device, a reduction of the threshold voltage $V_T$ is expected, while the opposite holds for p-MOSFETs. In addition, the presence of positive charge in the gate oxide causes additional Coulombic carrier scattering [11] and, hence, a reduction in the mobility and $G_m$ [11,17,18]. As shown elsewhere [16], the shifts observed in the single transistors can largely account for the performance changes in the circuit blocks, like a p-MOS buffer, under LHT γ-irradiation. Extensive tests have pointed out that the circuits will survive the expected total dose of the Herschel Mission [16].
Nevertheless, some peculiar phenomena, illustrated in Figs 7 and 8, have been found, which may require further studies. First, one can observe the conduction of the protection diode at 1 V reverse operation for the p-MOSFET of Fig. 7 under cryogenic operation conditions. This implies that, even before irradiation, this structure is not suitable for Electrostatic Discharge (ESD) protection purposes at LHT. Irradiation, either at room temperature or LHT, only aggravates the problem.

Fig. 7. Input characteristics corresponding to a 65 μm x 10 μm p-MOSFET before and after a 15 krd(Si) γ-irradiation at 7 K. A drain bias of -25 mV and -2.5 V was applied.

Fig. 8. Input characteristics of a 22 μm x 10 μm n-MOSFET before and after a 15 krd(Si) γ-irradiation at 7 K. A drain bias of 25 mV and 2.5 V was applied.

Another interesting phenomenon is represented in Fig. 8: transistors which show a subthreshold hump in the drain current before irradiation, no longer exhibit this after irradiation. The origin of the pre-irradiation subthreshold hump at 7 K is probably edge leakage along the LOCal Oxidation of Silicon (LOCOS) edges of the devices (a non-closed geometry was used). While the hump was not seen in the room temperature characteristics, it becomes obvious upon cooling. Recently, such a low-temperature effect has also been observed for more advanced isolation technologies,
like Shallow Trench Isolation (STI) [19,20]. The reason behind this is the different temperature coefficient of the $V_T$ for the main and the parasitic transistor. Normally, one expects that TID damage also increases the parasitic edge transistor leakage current in an n-channel transistor. This is related to the higher radiation-induced hole trapping in the thicker and low-quality field oxide, resulting in a lower $V_T$ at the LOCOS edges, compared with the main part of the channel [21,22]. The fact that here just the opposite is observed points to the specific nature of cryogenic radiation damage. A tentative explanation is that in the bird’s beak region of the LOCOS electron trapping occurs preferentially, which causes an increase of the corresponding $V_T$ and a disappearance of the edge leakage.

CONCLUSIONS

In summary, the device performance of 0.7 μm CMOS transistors and circuits is largely preserved after 15 or 30 krd(Si) $\gamma$-irradiation at 7 K. Some specific effects have been found, which once more emphasize the importance of cold radiation testing.

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SILICON-BASED CRYOGENIC ELECTRONICS: FROM PHYSICAL CURiosITY TO QUANTUM COMPUTING

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ABSTRACT

The research related to low temperature operation of materials and devices started more than 5 decades ago. Low temperatures are used for different reasons: to study fundamental material and device parameters, to enhance the performance of the devices, or because it is the natural operating temperature of some components (e.g. superconductors, single electron transistors, etc). Application fields are very broad including astrophysical, detectors and sensors, medical diagnostics, space, magnetic levitation transport systems, cryogenic instrumentation, etc. This paper aims to review the present status of silicon-based cryogenic electronics and to give an outlook related to the so-called emerging device technologies that are gaining in interest and are looking very promising for extending the ITRS roadmap. Special attention is given to dedicated cryogenic phenomena and to the increasing importance of quantization effects.

INTRODUCTION

Already since the early days of the semiconductor transistor, low temperature experiments have been used in order to get a better insight into the physical properties of the materials and devices. In 1949, Pearson and Bardeen [1] reported on the impact of the temperature on the behavior of boron and phosphorous in silicon, focussing on parameters such as drift, conductivity, mobility and Hall effect. Later on the interest in low temperature electronics, also referred to as cold or cryogenic electronics, was more driven towards applications such as e.g. high temperature superconductors, cryo supercomputers, infrared detectors, space applications, etc. Dependent on the success of the application field, which is also related to the availability of appropriate and cost-effective packaging technologies and cryo-coolers, the cryogenic research has known its up and downs. An overview of the different aspects of low temperature electronics, including physics, devices, circuits and applications can be found in a recently published book [2]. In recent years, there was a renewed interest in low temperature device operation due to the strong potential of so-called emerging technologies such as nano-electronics (e.g. single electron transistors), quantum computing and spintronics, which have a strong potential for extending the ITRS roadmap.

The low temperature range is mostly divided in three temperature regions related to the type of applications envisaged, i.e., the liquid nitrogen range (77 K) with a potential for commercial applications, the liquid helium range (4.2 K) for satellite communication, and the mK range for applications in the astrophysical world such as bolometers. The driving force for operating devices at lower temperatures is either the improved performance compared to conventional electronics (which is the case for most semiconductor-based devices) or the fact that some classes of devices only work...
at cryogenic temperatures, such as e.g. the superconductor-based components or some of the emerging silicon technologies that will be discussed later. Although strongly hampered by the required packaging technology, there has been a search for an optimal temperature range allowing the use of semiconductor/superconductor hybrid circuits.

Beneficial performance aspects of cryogenic operation include:
- increased mobility and saturation velocity of the carriers, leading to higher operation speed
- improved sub-threshold slope for MOSFETs
- reduced junction capacitance
- lower noise levels
- reduced junction leakage resulting in a lower power dissipation
- less temperature variation
- increased electrical conductivity resulting in shorter signal transmission times
- increased integration densities due to the increased thermal conductivity and the reduced operating voltages
- latch-up inhibition by a reduction of the gain of the parasitic bipolar transistors
- suppression of thermally activated degradation processes

Drawbacks of cryogenic electronics are:
- the requirement of the appropriate cooling systems
- selection of materials and processing modules that have to be optimized for low temperature operation
- packaging aspects
- dedicated test environments which are required
- interfacing aspects between ‘cold’ and ‘warm’ electronics
- availability of device and circuit simulators
- for some type of devices (e.g. SOI as will be discusses further) particular low temperature related phenomena are observed.

The behavior of the material and device parameters strongly depends on the selected temperature range, which on its turn is often dictated by the application field. For industrial oriented applications, much attention has to be given to handling, safety and cost aspects of the cooling systems. In the case of infrared focal plane arrays, it is sometimes sufficient to use passive cooling. This type of cooling would allow mobile systems. However, in most cases one has to use coolers based on cryogenic liquids such as oxygen (90 K), nitrogen (77 K), hydrogen (20 K) and helium (4.2 K). A real industrial breakthrough of cryogenic electronics was expected in the late 80-ties, where huge efforts were going on to develop a supercomputer operating at liquid nitrogen temperature. This ETA-10 computer, of which four commercial systems have been installed, contained 2000 chips with each 20 kgates and was operating at double speed compared to the room temperature computers [3]. Unfortunately, the parent company of the ETA Systems was demised in 1989.

Cryogenic electronics is also playing an important role in space missions [4-5], whereby use is made of a variety of components and circuits such as sensors, detectors, SQUIDs, superconducting tunnel junctions, CMOS readout electronics, etc. Table I summarizes the operating and the mission temperature for some future space flight missions [6]. Beyond the orbit of Mars, the average temperature seen by a spacecraft falls below the normal operating temperature range of the spacecrafts ‘standard’ electronics. There are two possible solutions to this problem. The spacecraft operating in the cold environment of deep-space can carry on board a large...
number of Radioisotope Heating Units to maintain an operating temperature for the electronics. However, these RHU’s are constantly producing heat so that a good temperature control becomes difficult [7]. Another approach is the use of cold electronics, which has the additional benefit of enhanced performance. Several far infrared detectors are only operating at cryogenic temperatures so that cold electronics will avoid possible interface problems. This approach also enables a possible implementation of semiconductor/superconductor hybrids. As the cold environment may also be hostile from a radiation viewpoint, it is essential to perform on earth cryogenic radiation testing [8].

<table>
<thead>
<tr>
<th>Mission</th>
<th>Operating Temperature</th>
<th>Mission Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Europa</td>
<td>-20 to +50°C</td>
<td>-170 to -50°C</td>
</tr>
<tr>
<td>Mars Sample Return</td>
<td>-40 to +50°C</td>
<td>-140 to +20°C</td>
</tr>
<tr>
<td>Pluto Flyby</td>
<td>-20 to +50°C</td>
<td>-235 to -100°C</td>
</tr>
<tr>
<td>Interstellar Travel</td>
<td>-20 to +50°C</td>
<td>-250 to -150°C</td>
</tr>
</tbody>
</table>

Table I: Operating and mission temperatures for future space flight mission [6].

This paper aims to give an overview of the trends in silicon-based low temperature electronics. Some special attention will be given to bulk and Silicon-on-Insulator (SOI) CMOS. Although design optimization for cryogenic operation is also very important, within the scope of this paper only technological and device architecture aspects will be discussed. It is essential to remark that for scaled-down technology nodes, quantization effects are very important. These will be even more pronounced at low temperatures. The implementation of SiGe layers has made it possible to achieve excellent cryogenic operation of bipolar type of devices. An outlook related to the cryogenic potential of emerging technologies such as single electron transistors, strained-Si devices, quantum computing and spintronics is included.

FUNDAMENTAL MATERIAL PROPERTIES RELATED TO DEVICE OPERATION

Recently, the authors published an in-depth overview of the behavior of the fundamental silicon parameters at low temperatures [9]. Key parameters are related to the charge transport, the mobility, the conductivity, the impact ionization coefficients, thermal properties, etc. These parameters will have a direct impact on some of the low temperature specific phenomena.

The transport properties of a MOSFET are influenced by the energy quantization in the inversion layer due to the confinement effect. At low temperatures the surface roughness and the Coulomb scattering will mainly determine the inversion layer mobility. In addition, for small geometry devices the impact of the high lateral electric field has to be accounted for. Balestra and Ghibaudo [10] have discussed this topic in more detail. The mobility will show up in the temperature behavior of the saturation velocity, which is illustrated in Fig. 1. The figure clearly demonstrates the performance improvement of low temperature operation. Besides the possibility for saturation velocity overshoot, due to ballistic transport, there is a strong increase in the saturation velocity at lower temperatures. For the same technology, a similar speed as for a 90 nm long device operating at room temperature is obtained for a 150 nm long device at 77 K. This statement is different than saying that a 90 nm technology node at room temperature has the same performance as a 150 nm
technology at liquid nitrogen. However, it clearly illustrates the fact that by cryogenic operation the need to scale down a technology node can be delayed by one generation.

![Figure 1: Velocity saturation of nMOS transistors versus channel length, at 300 K and 77 K [11].](image)

According to the ITRS roadmap, it is predicted that sub-10 nm gate length devices will be in production by 2016. At research level, the feasibility of such devices has already been demonstrated [12]. However, from a physical viewpoint the restriction in scaling is most likely to come from direct source drain tunneling. This implies that electrons in the source can due to thermal activation quantum-mechanically tunnel through the potential barrier beneath the gate and reach the drain region. The different types of conduction between source and drain are shown in Fig. 2a, i.e., thermally activated drift, thermally assisted tunneling and direct tunneling [13]. Thermally assisted direct tunneling will dominate when electrons in the source are thermally excited so that they can tunnel through the potential barrier near the drain. The threshold voltage for direct tunneling and thermally assisted tunneling depend on the temperature and the gate length [13]. Figure 2b shows the threshold voltage, defined as the voltage for a current of 1 nA/μm, as function of the temperature and the gate length. It can clearly be noticed that at high temperatures \( v_{th}^{\text{tunnel}} \) is higher than \( v_{th}^{\text{thermal}} \). For decreasing temperatures both first become equal to each other before the direct tunnel component is dominating over the thermally activated tunneling. This implies that dependent of the gate length there is a crossover temperature \( T_C \) whereby both mechanisms are equal. As seen in figure 2b, this temperature is equal to 130, 50 and 25 K for a gate length of 8, 25 and 52 nm, respectively. In other words, the physical gate length for which direct tunneling occurs is larger for cryogenic operation compared to room temperature operation. The given calculations are for structures with an electrical variable junction depth, fabricated along the inversion layer drain (ILD) concept and making use of conductive spacers. A similar theoretical analysis for MOSFETs with a rectangular potential distribution pointed out that the minimum channel length at 300 K changes from 8 to 6 nm [13], an observation which is important for determining the limits of the gate length for low voltage/low power operation of digital circuits.
Figure 2: (a) Three possible conduction mechanisms between source and drain of short channel devices. (b) Calculated threshold voltage for direct tunneling (solid lines) and thermally activated tunneling (dotted lines) as a function of temperature for a gate length of 8, 25 and 52 nm, respectively. The arrows indicate the crossover temperature [13].

Another important material parameter strongly influencing the low temperature behavior is the impurity freeze out. While still moderate at 77 K, impurity freeze out will dominate below 20 K, especially in lowly doped device regions. For a general treatment of the subject one has to take into account the temperature, the electric field, and the doping concentration. Also the type of doping (i.e., B, P, As, B, In....) has an impact [14]. The effect will become very pronounced in lowly doped drain (LDD) regions, which are a standard process option for deep submicron technologies in order to reduce the short channel effect and to control hot carrier effects. The carrier freeze out of the LDD region will increase the series resistance [15].

Impact ionization is a key phenomenon for device operation at low temperatures, as reviewed by the authors [16]. The ionization rates for electrons ($\alpha_e$) and holes ($\alpha_h$) are dependent on both the electrical field and the temperature and have been rather well modeled down to 77 K. Although both rates increase for decreasing temperatures, the ratio ($\alpha_e/\alpha_h$) is decreasing as illustrated in Fig. 3. This means that the dispersion between the two coefficients is decreasing as function of the temperature, an effect which is becoming more pronounced for higher electrical fields. At temperatures below 10 K the dominant ionization mechanism is shallow-level impact ionization due to the electric field assisted ionization of frozen-out shallow dopants.

Important phenomena, observed in CMOS devices and related to impact ionization and the associated multiplication current, are the kink effect, latch and latch-up, transient and hysteresis effects, and excess low frequency noise [16]. Some of them are further briefly discussed. Although the kink effect was first observed in SOS and later in SOI devices (see e.g. [18] for an overview), also bulk CMOS transistors operating at 4.2 K may suffer from it as illustrated in Fig. 4a [19]. In the kink region there is a strong increase in drain current for a small increase of the drain-source voltage. The amplitude of the kink can be reduced by using a lowly doped drain (LDD) region. It has been well established that there is an excess low frequency noise component associated with the kink [20]. Quite often, the devices suffer from transient and hysteresis effects. All these effects have been studied in detail and are nowadays well understood.
Figure 3: Theoretical ($\alpha_n/\alpha_p$) ratio as a function of temperature, taking into account the electrical field. Some experimental data for $E=250$ kV/cm from [17] are also included.

Figure 4: (a) Illustration of the kink effect in a 10 $\mu$m x 5 $\mu$m n-MOSFET at 4.2 K, processed in the substrate with (dashed lines) and without LDD (full lines). (b) At 2 V a 1/f spectrum is observed, while the kink-associated excess low frequency noise ($V_{DS}>3.4$ V) has a Lorentzian spectrum (20x20 $\mu$m MOST operating at 4.2 K) [20].

SILICON-ON-INSULATOR (SOI) TECHNOLOGIES

Several of the impact ionization related effects (kink, hysteresis, transients, excess noise, etc) are very pronounced in partially depleted (PD) SOI devices due to the floating body effect. These may be overcome by using grounded body ties [21], fully depleted (FD) SOI devices [22], or special structures such as e.g. twin-gate designs [23] and dual gate SOI MOSFETs [24]. For a grounded body tie it may be necessary to work with multiple contacts in order to reduce the series resistance at low temperatures. In the case of a twin gate, the ratio of the gate length of the 'master' to the gate length of the 'slave' transistor is an important factor. The higher the ratio, the better the kink suppression. The authors have published in 1999 a review on the potential of SOI for cryogenic operation [25].
Even when the impact ionization effects are suppressed, the SOI devices still remain very prone to pulses applied to one of their terminals, i.e., source, drain, front- and back-gate. When applying a pulse to the front- or back-gate of an SOI transistor, carriers have to be supplied in order to evolve to the steady state. Especially in weak inversion and at small drain bias, where the supply of carriers from the source is limited, generation-recombination processes will dominate the measured channel current transients. The associated time constants are more pronounced for lower bias. The transient effects can be used to determine the minority carrier lifetime [26] and have an effect on the circuit performance. Figure 5 shows drain current transients measured for an nMOST after “switching-off” its front-gate from different \( V_{FG,\text{high}}>0.1 \text{V} \) values to \( V_{FG,\text{low}}=0.1 \text{V} \) [27]. For \( V_{FG,\text{high}} \) lower than 1.1 V the well-known \( I_D \) undershoot arises until the steady-state condition is reached by means of hole generation. Generated holes fill the space-charge region between the maximum depletion width, corresponding to \( V_{FG,\text{high}} \) and the steady-state depletion width associated with \( V_{FG,\text{low}} \). For low \( V_D \), these holes can be supplied by four different mechanisms: bulk generation in the space charge region, source/drain to film space-charge regions, and generation at front and back interfaces.

![Figure 5: Normalised \( I_D \) “switch-off” transients from different front-gate voltage \( V_{FG,\text{high}} \) values to \( V_{FG,\text{low}}=0.1 \text{V} \) measured for an \( L=W=10 \mu\text{m} \) nMOST at \( V_D=25 \text{mV} \) [27]. \( I_D(t=\infty) \) = steady state \( I_D \) current level at \( V_{FG}=V_{FG,\text{low}}=0.1 \text{V} \).](image)

The time constants drastically increase upon cooling and can become even hours at 77 K [28]. In the latter case the transients are so long that the device can be switched to a metastable charge state. This is then forming the basic concept of the so-called Multistage Charge Controlled Memory Effect (MCCM) [29]. This phenomenon can be successfully used for the development of single transistor memories [30]. In principle, these devices can be considered as a type of precursor for the single electron transistors that will be discussed in a later section. For standard transistor dimensions the size of the ‘charge cavity’ is so large that it contains more than one electron. Essential for these type of devices is the ‘history’, implying that the reaction to a voltage pulse will depend on the previous charge state of the component and the time elapsed between different charge pulses. It is also important to remark that due to the rather slow transistor response at low temperatures, the determination of the different performance parameters, such as e.g., threshold voltage and sub-threshold slope, becomes more difficult and may require special techniques [31-32].

Applying bias during the cooling down of the devices may restrict some of these artifacts. However, subsequent bias pulses again aggravate the situation.

For scaled downed technologies, quantization effects have to be taken into account. First there is the fact that for deep submicron devices, one has to account for the quantization of the inversion layer [33-34]. The presence of high vertical electric fields, depending on the gate voltage and film doping concentration, may lead to a band splitting. The major consequences are an increase of the bandgap at the interface, whereby for an nMOST the first allowed energy level is shifted by an amount $\Delta E$ above the conduction band minimum in the body. This has an impact on the threshold voltage $V_{TH}$. In addition, the electrical gate oxide thickness becomes higher than the physical one, due to the peaked distribution of the charge density in the 2-dimensional electron gas (2-DEG). This results in a gate voltage dependent effective oxide thickness and gate capacitance. As a consequence, also the 2-DEG charge density and the drain current $I_D$ are modified by quantization. These quantization effects also have a strong impact on the low frequency noise modeling [35].

For thin film SOI devices, the classical expression of the threshold voltage versus the film thickness has to be adjusted as soon as the film thickness is below a critical value due to the occurrence of two-dimensional subbands. The quantization of the short-channel effect (SCE) occurs for a film thickness below 5 nm and is related to an increase of the effective bandgap energy and the decrease of the effective density of states, resulting in an increase of the majority carrier extension [36]. The quantization effects are more severe in surface channel than in buried channel SOI MOSFETs as the larger energy bandgap results in a larger depletion width with the increasing built-in potential. Low temperature operation makes the quantization more pronounced as illustrated in Fig. 6. This figure gives a representative parameter to study SCE, i.e., the drain voltage derivative of the threshold voltage $\gamma=(dV_{TH}/dV_D)$ [37]. The $\gamma$ increase for lower temperatures is caused by a decrease of the effective density of states, leading to a decrease of the Debye length. According to the classical theory the Debye length is expected to increase with decreasing temperature.

![Figure 6: Temperature dependence of the drain-voltage derivative of the threshold voltage ($\gamma$) for 0.1 $\mu$m pMOSFETs on SIMOX with an 8 nm silicon film [37]. The experimental points are the average values for 5 measured devices.](image-url)
Quantization effects also influence the transport properties in the silicon film resulting in a modification of the transconductance. Local thickness variations may lead to oscillations in the transconductance, whereby the oscillation period is determined by the size of silicon islands or quantum dots in the channel [38].

A new phenomenon, called "Linear Kink Effect", has recently been observed in bulk nMOSTs operating at 4.2 K or at room temperature if a high value resistor is connected in series [39]. The effect is characterized by a second peak in the transconductance, as illustrated in Fig. 7a for an nMOST. For SOI devices the effect is already occurring at room temperature, both in partially and fully depleted devices [40]. For the latter the effect is more pronounced for an accumulating back-gate voltage, as shown in Fig. 7b. At 77 K the peak becomes larger and changes its shape [41].

Associated with the LKE in the drain current is a strong increase of the low-frequency noise spectral density $S_n$, similar as for the impact-ionization related noise overshoot discussed above. The parameters (plateau value and time constant) of the excess Lorentzian noise, which is generated by RC filtered shot noise associated with both the electron valence band (EVB) tunneling current and the forward source-body current, has been studied in detail for both partially and fully depleted devices [42-43]. It has to be remarked that the LKE occurs for higher gate voltages compared to the 'standard' kink. At the same time, it is observed that for a gate voltage above the LKE threshold, a change in the nature of the switch-off transients in the drain current takes place (see Fig. 5). For voltages below the LKE the transients are negative, while they become positive for higher front gate voltages.

A model based on electron valence band (EVB) tunneling, whereby the injection of majority carriers leads to a forward biasing of the body-source junction, has been proposed to explain the experimental observations [40]. This model is schematically illustrated in Fig. 8.

Figure 7: Linear Kink Effect observed in (a) a bulk n-MOSFET at 4.2 K and at 300 K with a 10 GΩ resistance connected to the substrate [39], and (b) a fully depleted SOI n-MOSFET (at $V_{BG}=5$ V to -20 V) operating at room temperature and at 77 K [41].
n-MOSFET diagram and gate tunneling mechanisms in an ultra-thin gate oxide n-MOSFET: Valence Band and Conduction Band Tunneling [40].

Initial results on the low temperature operation of advanced SOI technologies using high-\(k\) dielectrics and metal gate are becoming available [44]. Figure 9 illustrates for FD-SOI devices with a HfO\(_2\) gate dielectric and TaSiN gate electrode the temperature dependence of some electrical parameters like the threshold voltage, the swing and the low field electron mobility. It can clearly be seen that for lower temperatures the threshold voltage increases, while the swing decreases. Below 200 K the mobility tends to saturate, as surface and Coulomb scattering are becoming the dominant mechanisms. For narrow channel devices the saturation is occurring at higher temperatures and lower values due to the impact of the sidewall scattering.

![Figure 8: Band diagram and gate tunneling mechanisms in an ultra-thin gate oxide n-MOSFET: Valence Band and Conduction Band Tunneling [40].](image)

![Figure 9: (a) Front threshold voltage and swing and (b) front-interface low field mobility for PD SOI devices with a HfO\(_2\) gate dielectric and a TaSiN gate electrode [44]. The impact of the channel width on the mobility is clearly shown.](image)
Silicon bipolar devices have for a long time been considered as not suitable for low temperature operation because of i) the exponential decrease in current gain with temperature due to the heavy-doping induced bandgap narrowing in the emitter, ii) the increase in base resistance with cooling due to freeze out, and iii) the decrease in frequency response due to the lowering of the carrier diffusivity [45]. However, acceptable operation in the 77 K range can be obtained by an optimization of the doping profiles [46]. The real breakthrough of heterojunction bipolar transistors (HBTs) for cryo application was achieved by using epitaxial SiGe alloys, due to the possibility for bandgap engineering of the base whereby the Ge-induced band offsets exponentially compensates the bandgap narrowing of the emitter. Cressler [47] has recently reviewed this topic and the improvement in current gain over the years is shown in Fig. 10. SiGe optimized HBT technologies are capable to achieve current gains higher than 500, peak cutoff frequencies in excess of 60 GHz and unloaded ECL gate delays as low as 22 psec at 77 K [48]. Figure 11a and b show for a 77 K optimized emitter cap SiGe HBT the Gummel characteristics at 300 K, 77 K and 5.84 K and the current gain as a function of the temperature [49].
The excellent low temperature performance of SiGe technologies also offers the possibility to use a SiGe BiCMOS technology aiming at high-speed cryogenic applications. The use of SiGe has no direct impact on the radiation hardness of these technologies, making it a good choice for rf systems on a chip (SOC) operating in a radiation environment [50]. Recently, it has been reported that the inherently good total ionizing dose tolerance at room temperature even improves with cooling down to 77 K, allowing irradiation levels up to 1 Mrd [51].

EMERGING SILICON TECHNOLOGIES

In order to keep up with the ITRS roadmap and to enable the industrial fabrication of sub 10 nm technology nodes by 2016, huge investigations are required to circumvent the 'red brick wall' and to overcome the physical, technological and economical roadblocks [52]. Therefore, the ITRS roadmap updates every two years are also giving more and more attention to the so-called emerging device technologies. Some of them with their natural operating temperature in the cryogenic range will be briefly addressed.

A main problem for deep submicron CMOS devices is the mobility degradation which is worse for smaller device geometries. In addition, the use of high-k gate dielectrics shifts the mobility further away from the universal mobility curve. Improvement of both electron and hole mobility can be achieved by using SiGe layers and/or strained Si or Ge [53-56]. The explanation, i.e., role of coulomb scattering, inter-valley phonon scattering and surface roughness scattering, for the impact of strain on the mobility is still under discussion due to the discrepancy between theoretical and experimental results. Important, however, are the observations that the operating temperature has an influence on the mobility, as illustrated in Fig. 12 for standard Si devices. Figure 13 shows the temperature dependence of the stain-induced mobility enhancement in n- and p-FETs [57]. A $T^{-1.9}$ law would point towards a phonon-limited mobility, while the observed $T^{-1.2}$ dependence indicates that there is a contribution of the Coulomb scattering caused by a reduction in the average effective mass. A further step could be the use of bulk Ge or Ge-on-Insulator (GeOI) as Ge has at room temperature a 2x higher electron and a 4x higher hole mobility compared to Si.

![Electron and hole mobility](image-url)

**Figure 12:** Electron (a) and hole mobility (b) of Si devices as function of the effective electric field, measured at 83, 103, 123, 143, 163, 183, 203 223, 273 and 300 K [57]. The dotted line indicates the universal mobility curve as 300 K according to Takagi et al. [58].

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By scaling down the device channel length one obviously has to take into account some specific transport phenomena. First, one has to deal with the ballistic transport of the carriers. As soon as the channel length is becoming less than the carrier mean free path, no collisions are limiting the carrier mobility so that a strong increase in current is observed. These devices are operating based on thermo-ionic emission (limiting the source velocity) and quantum tunneling and are characterized by the fact that the current is limited by the electron supply at the source [59-60]. For smaller geometries so that one obtains silicon islands between source and drain, the Coulomb blockade effect becomes important. In a single electron transistor (SET) the electrons tunnel to isolated silicon island and remain confined there. If the electromagnetic environment around the island has a high impedance then the charge on the island will be well defined. The localized electron will block the current flow over a significant range of the applied voltage. The working principle is schematically illustrated in Fig. 14a [61], giving a typical voltage-current characteristic. The length of the Coulomb gap $-V_C < V < +V_C$ is temperature dependent as shown in Fig. 14b [62]. A second condition for SET operation is that the electron states on the island are energetically separated by the electron charging energy $e^2/2C$, which must be larger than the thermal energy $kT$. $k$ is the Boltzmann constant and $C$ the capacitance. Therefore the maximum operating temperature can be calculated as

$$T \ll e^2/2kC$$

Figure 13: Temperature dependence of the effective mobility at an electric field $E_{eff} = 0.6$ MV/cm [57].

Figure 14: (a) current-voltage characteristic showing a Coulomb gap for $-V_C < V < +V_C$ and the tunnel possibility [61]. (b) Illustration of the temperature dependence of the Coulomb blockade [62].
Related to SETs are the Resonant Tunneling Diodes (RTDs) which are also fabricated in silicon/germanium based materials [63]. These two-terminal devices are integrated with MOSFETs in order to enable circuit functions at higher speed with fewer devices. A further step is going to quantum computing. In that case the devices are relying on the phase information of the quantum wavefunction to store and manipulate information. The wave information of any quantum state is called a qubit and is very sensitive to the environment. In principle a qubit is similar to a 'bit' in the conventional computing. For the implementation of quantum computers different approaches are being pursued: i) bulk resonance quantum implementation including nuclear magnetic resonance, ii) atomic implementation including trapped ions and optical lattices, and iii) solid state implementation including semiconductors and superconductors. The solid-state approach is the most promising for achieving quantum computers with e.g. $10^6$ qubits.

Some basic principles of quantum computing in silicon are briefly discussed [64]. In silicon, the electron wavefunction at the nucleus extends over a large distance through the lattice. Two nuclear spins can interact with the same electron, resulting in electron-mediated or indirect nuclear spin coupling. As the electron is sensitive to an external applied electric field, the hyperfine interaction can be controlled by the voltage applied to the gate of the device, thereby enabling the external manipulation of the nuclear spins. A special case arises if the nuclear spin is located on a positively charged donor such as e.g. P in Si. A quantum computer then consists of a large array of donors located beneath the surface of the silicon host lattice. A quantum mechanical calculation is performed by the control of three different parameters: i) the gates above the donors control the strength of the hyperfine interaction and thus the resonance frequency of the nuclear spins underneath them, ii) the gates between the donors turn on and off the electron-mediated coupling with the nuclear spins, and iii) an external applied a.c. magnetic field flips nuclear spins at resonance. A schematic illustration of the working principle is given in Fig. 15. The adjustment of the coupling between the spins and the interaction with the magnetic field are at the basics of the computation. $^{31}$P is a shallow donor in Si with a spin $=1/2$. At sufficient low concentrations and temperatures around 1.5 K, the electron spin relaxation time is more than 10 hours. At mK temperatures the phonon limited relaxation time is of the order of $10^8$ seconds [65], which is very suitable for quantum computing. Irreversible interactions between the nuclear and the electronic spin should be avoided. It is important to remark that a quantum computer is non-dissipative and therefore operates well at low temperatures.

The future of these different emerging technologies is unclear although several of the investigated devices have a strong potential. Especially for memory type components, the use on non-standard concepts may become a necessity in order to achieve high densities. This is illustrated in Fig. 16 for the expected evolution of bit-addressable memories [66]. In order to go further than 64 Gb integration (density of about 10 Gb cm$^{-2}$) ultra small geometries must be used to solve the problems with the storage capacitance. For room temperature operation, non-volatile random-access memories (NOVOAM) may be a good alternative to bridge the gap, opening the perspective for terabit-scale integrated circuits. The investigations towards room temperature operation of SET-FET hybrid circuits are very promising and may be the long term solution.
Figure 15: Illustration of two cells in an array containing $^{31}\text{P}$ donors and electrons in a Si host, separated by a barrier from metal gates on the surface [64]. The $A$-gates control the resonance frequency of the nuclear spin qubits, the $J$-gates control the electron-mediated coupling between adjacent nuclear spins. The ledge over which the gates cross localizes the gate electric field in the vicinity of the donors.

Figure 16: Integration expectations for bit-addressable memories [66]. The solid line labeled ‘DRAM’ is according to the ITRS roadmap. The bit density is calculated using a log-linear extrapolation similar to that used in the roadmap (1.5 chip area increase per technology node). Open points and dashed lines indicate problems with no known solution. Dotted lines show SET/FET hybrids that require cooling down to the indicated temperatures.

CONCLUSIONS

The field of cryogenics has been reviewed, going from fundamental device physics to state-of-the-art device research. Beside some specific application fields, such as e.g. astrophysics and deep-space missions, also several of the emerging devices associated with the end of the ITRS roadmap, having a strong potential are relying on low temperature operation.
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LOW-TEMPERATURE PERFORMANCE OF ULTIMATE SI-BASED MOSFETs

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Abstract

Experimental results for low and high temperature operation are presented for advanced bulk-Si and fully-depleted SOI (FDSOI) MOSFETs with mid-gap metal gate and high-k gate dielectric. The results are rather similar to those previously obtained in more classical SOI devices in terms of threshold voltage, swing, transconductance or mobility. Moreover, the effective mobility of HfO$_2$ n- and p-MOSFETs fabricated on bulk Si has been investigated using low-temperature measurements and constant-voltage stress. It was found that Coulomb scattering mechanism has a significant influence on mobility degradation. A correlation between trapped charge and mobility degradation has been made, which can explain the difference observed in mobility behavior in HfO$_2$ nMOS and pMOS as compared to SiO$_2$ devices.

Introduction

As stated by the ITRS roadmap, further miniaturization of CMOS technologies will require the use of high-k gate dielectrics and metallic gate electrodes. This will allow a strong reduction of gate tunneling current, poly depletion effect, poly doping penetration, and gate access resistance. Hafnium oxides have been shown to be promising candidates as high-k dielectrics (k $\approx$ 25) with poly and metal gates (1-3). However, the interface and bulk oxide quality are not as good as for the SiO$_2$ system. This may influence the gate leakage current and mobility behavior. The mobility degradation was observed by many authors (3-4), but the background mechanisms are still controversial. In this paper, the effective mobility is extensively investigated on CMOS devices with a metal gate and HfO$_2$ gate dielectric on top of a SiO$_2$ buffer layer. More specifically, we study Coulomb scattering contribution to mobility degradation, using low-temperature measurements and constant-voltage stress (CVS).

From a different angle, conventional scaling of bulk-Si MOSFETs is becoming more and more difficult. Ultra-thin fully-depleted Silicon-On-Insulator (FDSOI) device is a promising candidate for further scaling while still maintaining conventional processing techniques. High performance FDSOI devices using undoped channel have been demonstrated, achieving correct threshold voltages by the use of a mid-gap gate material,
either by total silicidation of the poly Si gate (5-7) or by the use of TiN (8) or TaSiN metal gates (9). The combination of mid-gap gate and undoped channel provides the benefits of suppressing the polysilicon depletion and increasing the effective carrier mobility by significantly reducing the vertical electric field. It also reduces threshold voltage variations with silicon film thickness. Thin film FDSOI devices with undoped channel, metal gate and high-k dielectric are therefore very attractive to maintain low gate leakage and control short-channel effects. Such devices, however, still need a better understanding of carrier transport at the high-k interface and in the ultra-thin film. In this paper, we review the major mechanisms involved in n-channel thin film FDSOI devices with high-k and metal gate at low and high temperature, ranging from 10 K to 450 K.

A- BULK DEVICES WITH TiN/HfO₂/SiO₂ GATE STACK

A.1. Experimental Details

The technology consists of a Damascene replacement gate process with CVD TiN/W, and, for the gate dielectric, HfO₂ films deposited by ALCVD using an Atomic Layer Deposition PULSAR™ system (ASM/Microchemistry). The HfCl₄ and water were used as precursors. The thin films of HfO₂ were deposited on 0.7 nm native chemical SiO₂ oxide and annealed at 600°C (PDA1) and 800°C (PDA2) in Nitrogen. More details about the process can be found elsewhere (10). Table 1 summarizes the characteristics of the various HfO₂ splits and reference SiO₂ sample investigated. Two values of HfO₂ film thickness were available, 3.5 nm or 4.5 nm. The resulting EOT's, extracted from C(V) data with Poisson-Schrodinger simulations, range between 1.35nm and 2.3nm. The higher post deposition anneal (PDA) temperature gives rise to a re-oxidation of the interfacial oxide, which increases the final EOT. The studied devices are large 100x100μm² nMOS and pMOS transistors.

<table>
<thead>
<tr>
<th>Sample No</th>
<th>HfO₂ dep</th>
<th>PDA T°C</th>
<th>EOT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4.5 nm</td>
<td>600</td>
<td>1.65nm</td>
</tr>
<tr>
<td>2</td>
<td>4.5 nm</td>
<td>800</td>
<td>2.27nm</td>
</tr>
<tr>
<td>3</td>
<td>3.0nm</td>
<td>800</td>
<td>1.9nm</td>
</tr>
<tr>
<td>4</td>
<td>3.0nm</td>
<td>600</td>
<td>1.35nm</td>
</tr>
<tr>
<td>5</td>
<td>Ref SiO₂</td>
<td></td>
<td>2.6nm</td>
</tr>
</tbody>
</table>

Table 1: Characteristics of different HfO₂ splits and reference SiO₂ samples.

A.2. Results and Discussion

Effective mobility split C-V measurements, performed on n- and p-MOSFETs, are shown in Fig 1. According to previous findings (3-4), we observed mobility degradation at room temperature for electrons, but not for holes. These split C-V curves exhibit a drop at low field, which can be attributed to Coulomb scattering phenomenon, but also to a systematic error of the split C-V technique. This drop can be further enhanced by a C-V threshold voltage dispersion with frequency, due to interface traps. To avoid this problem, we preferred to use in this work effective mobility curves extracted from Iₐ(Vₜ) measurements as (11):
\[
\mu_{\text{eff}}(V_g) = \frac{L}{W} \frac{I_d(V_g)}{C_{\text{ox}}(V_g - V_t)V_d} = \frac{\mu_0}{1 + \theta_1(V_g - V_t) + \theta_2(V_g - V_t)^2}
\]

where \(\mu_0\) is the low-field mobility and \(\theta_1\) and \(\theta_2\) are mobility attenuation factors.

In order to gain more insight into the mobility mechanism, we applied this method at various temperatures ranging from 4.2K to 300K (Fig 2). In addition to the increase in effective mobility due to the decreased phonon scattering, nMOS HfO\(_2\) devices were found to have a bell shaped behavior versus inversion charge at low temperature that is often associated with dominant Coulomb scattering.

Figure 1: Effective mobility \(\mu_{\text{eff}}\) versus effective electric field \(E_{\text{eff}}\) for NMOS (a) and PMOS (b) transistors on bulk Si; all HfO\(_2\) splits (1-4) are compared to the reference SiO\(_2\) sample (5).

Figure 2: Effective mobility \(\mu_{\text{eff}}\) versus inversion charge at low temperatures for HfO\(_2\) nMOSFET (a), HfO\(_2\) pMOSFET (b), and SiO\(_2\) reference nMOSFET (c).
This rounding of the curves can be interpreted as a negative $\theta$ factor in equation 1. Surprisingly, pMOS devices did not exhibit such bell shaped behavior, like the SiO$_2$ n and pMOSFETs, even if the low field mobility is still increased.

Compared to SiO$_2$ samples, the increase in electron and hole effective mobility with decreasing temperature was found to be much weaker in HfO$_2$ samples, as exemplified in Fig 3. This could be due to a more pronounced Coulomb scattering to mobility degradation in HfO$_2$ samples.

![Figure 3: Low-field mobility variation at low temperature: a) electron mobility for HfO$_2$ sample 1 and SiO$_2$ sample 5, b) hole mobility for sample 3 and 5.](image)

The influence of Coulomb scattering on effective mobility has been investigated using constant voltage stress (CVS). $I_d(V_g)$ curves were measured at several steps of the CVS, which enabled us to extract the effective mobility. The amount of created interfacial ($N_{it}$) and bulk ($N_{ct}$) traps are obtained using Winokur's technique (11-12). This method is a convenient way to extract $N_{it}$ and $N_{ct}$ from $I_d(V_g)$ curves, but makes the assumption that interface traps in the upper half of the band gap are of acceptor type and those below are donors. Furthermore, this method can't accurately extract interface trap densities below $10^{11}$ cm$^{-2}$ eV$^{-1}$. Interface and bulk oxide trap densities are given by:

$\Delta N_{it} = \frac{C_{ox}}{q}(\Delta V_I - \Delta V_{mg})$  

and

$\Delta N_{ct} = -\frac{C_{ox}}{q}\Delta V_{mg}$

where $\Delta V_I$ and $\Delta V_{mg}$ are respectively the threshold and mid-gap voltage shifts during the stress. These gate voltages are found for $\psi_s = 2\phi_f$ and $\psi_s = \phi_f$ respectively, from the following equation (13):

$$I_d(V_g) = -\frac{W}{L} \mu_0 \left(1 - \exp(-\beta V_d)\right) \left(\sqrt{Q_d(\psi_s)^2 + \frac{4q\varepsilon_s n_i^2}{\beta N_A} \exp(\beta \psi_s)} - Q_d(\psi_s)\right)$$

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\( \psi \) being the surface potential, \( \beta = q/k_BT \), \( \mu_0 \) the low-field mobility, \( \varepsilon_{si} \) the silicon permittivity, \( n_i \) the intrinsic concentration and \( Q_d \) the depletion charge.

Rather long (1000 seconds) CVS has been performed on n and pMOSFETs for both gate injection and substrate injection \((V_g = \pm 3 \text{ V})\). The result for a nMOS-sample 1 with substrate injection is shown in Fig 4. The bell shape behavior of the curve is enhanced with injected electron density. This effect is related to an increasing negative \( \theta_i \) value, as shown by the inset of Fig 4. The slope of the reciprocal mobility \( \mu_0^{-1} \) with oxide charge build-up \( \Delta N_{ox} \) yields the Coulomb scattering coupling parameter \( \alpha \) [14]. This parameter was found to be slightly higher in the HfO\(_2\) films with thin interfacial oxide layer, i.e. low PDA temperature (see Fig. 5). This suggests that the mobility degradation is likely due to remote Coulomb scattering by charges located beyond the buffer oxide and residing mostly in the volume and at the interfaces of the HfO\(_2\) dielectric.

![Figure 4: Electron effective mobility versus inversion charge for sample 1, with injected charge density ranging from 0 to \(10^{21} \text{ cm}^{-2}\). The inset shows the variation of the mobility attenuation factor \( \theta_i \) during stress.](image)

![Figure 5: Reciprocal low-field mobility variation versus bulk charge variation during stress, for nMOSFETs HfO\(_2\) samples 1-4 (substrate injection). The slope \( \alpha \) is related to Coulomb scattering mechanism.](image)

The bulk trapped charge, calculated with Winokur’s method are shown in Fig 6 for nMOSFETs. Interfacial trap density is not shown as it exhibited the same behavior for low or high density of injected charge. The nature of the bulk trapped charge was found to depend mostly on the injecting electrode. A positive charge was induced by gate injection (Fig. 6b), that we attributed to a prevailing anode hole injection process into the HfO\(_2\) layer; indeed, the amount of trapped charges seems to be enhanced for a thin buffer SiO\(_2\) layer thickness. For substrate injection (Fig. 6a), we found negative charges, probably due to electron trapping into the HfO\(_2\) bulk. These charges originate from electron that tunnel either into the HfO\(_2\) conduction band or bulk electron traps. Concerning the interface charge density, it should be noted that the method used in this work gives them a negative charge for nMOSFETs (resulting from filled acceptor traps), and a positive charge for pMOSFETs (resulting from emptied donor traps).

A correlation can be made between the trapped charges and the mobility degradation. A behavior such that of Fig 4 has been observed only for substrate injection for nMOS devices, and for gate injection for pMOS devices, while negligible mobility degradation was observed when injection is made from the other electrodes. It is worth noting that the bulk and interface charges are of opposite sign for that case. As the bulk trapped charge
mostly resides in the HfO$_2$ volume, we suppose that the bulk charges can be screened by the interface traps when they are of opposite sign, resulting in a reduced Coulomb scattering contribution to mobility degradation. As a result, this mechanism could be responsible for the attenuated mobility degradation observed in pMOSFETs of Fig 1b, provided that the HfO$_2$ layer exhibit native negative bulk charges.

Figure 6: Bulk charge density variation, determined from Winokur’s method, with injected electron density from (a) the substrate with $V_g = +3$ V and (b) from the gate with $V_g = -3$ V.

B- FD SOI DEVICES WITH METAL GATE AND HIGH-K GATE OXIDE

B.1. Technological Details

The devices were fabricated at Motorola DNA on standard UNIBOND® SOI wafers with a silicon film thickness of 110 nm and a buried oxide thickness of 200 nm. The superficial silicon was thinned down to 20 nm by successive thermal oxidation and oxide wet-etch. The transistor channel was left undoped with a p-type background concentration $N_A \approx 10^{15}$ cm$^{-3}$. Shallow trench isolation was used. HfO$_2$ gate dielectric was deposited by MOCVD at 550°C, resulting in a 12Å interfacial layer and a 35Å HfO$_2$ dielectric stack (Fig.7).

Figure 7. TEM of the channel and the gate oxide.

TaSiN was then reactively sputtered to form the gate electrode. A nitride liner was
deposited and, after HfO2 removal from the source/drain regions, a 30-nm-thick selective 
epitaxial silicon was grown at 800°C in the extension regions. After gate patterning, P+ 
was implanted in the extensions. Cobalt silicidation and copper backend processing were 
used. After completed processing, the silicon film thickness in the channel was 
approximately 15 nm. A cross-section TEM of the final device is illustrated in Fig.8.

B.2. Low and High Temperature Measurements

Front gate characteristics

Figures 9a and 9b show the drain current and the transconductance characteristics at 
V_D = 0.1 V for high and low temperatures. As temperature decreases from 300 K to 50 K, 
the current increases by 64 % and the peak of transconductance by 95%. Below 50 K, 
both saturate or slowly decrease. By contrast, from 300K to 475K, the current decreases 
by 36 % and the g_m peak by 40 %.

Figure 9. Drain current (a) and transconductance (b) versus gate voltage for various 
temperatures (SOI MOSFET).

![Drain current characteristics for high drain voltage (V_D = 1.5 V) and different temperatures.](image)

Figure 10. Drain current characteristics for high drain voltage (V_D = 1.5 V) and different temperatures.

![Low temperature measurements of the gate current.](image)

Figure 11. Low temperature measurements of the gate current.

For V_D = 1.5 V, the current increases by 49 % between 300 K and 50 K and decreases 
by 30% between 300 K and 475 K. Below 50 K, it slowly decreases (Fig. 10). The drain
current leakage increases by about three orders of magnitude between 15 K and 475 K at $V_G = -0.5$ V. The gate current is very low ($= 10^{-12}$ A/$\mu$m$^2$ for $V_G - V_T = 1$ V and 300 K) and decreases by one order of magnitude between 300 K and 15 K (Figure 11).

**Back gate characteristics**

The high temperature back-gate measurements confirm the previous results. For $V_D = 0.1$ V, the drain current (Fig. 12.a) and the transconductance peak (Fig. 12.b) decrease by 46% and 48% respectively as the temperature increases from 300 K to 475 K. Similar variations are obtained at $V_D = 1.5$ V.

![Figure 12. High temperature back-gate measurements of the drain current (a) and the transconductance (b).](image)

**B.3. Discussion**

**Front gate**

As shown in Fig. 13, the threshold voltage is relatively high for undoped devices (0.3 V at 300 K) thanks to the mid-gap gate metal. It increases quasi-linearly with lowering the temperature (Fig. 13) with a slope of -0.8 mV/K. This value is very similar to previous measurements on thin film SOI devices and well below the values obtained in bulk devices ($= -2$ mV/K) (15). The subthreshold slope is rather ideal (60 mV/decade at 300 K), indicating a good quality front interface with a very low interface trap density (Fig. 13). As expected, the swing decreases linearly for lower temperature, with a slope of -0.2 mV/decade. Below 25 K, it saturates probably due to the influence of the interface traps, as the Fermi level approaches the conduction band edge.

The low field mobility ($\mu = 225$ cm$^2$/Vs at 300 K), extracted from the maximum of the transconductance, is reasonable and increases with decreasing temperature (Fig. 14). Indeed, the phonon scattering effects decrease, hence resulting in a higher mobility. For temperatures higher than 200 K, the mobility variation is in proportion to $T^{-1.2}$, very close to previously observed dependences $T^{-1.5}$. This indicates that phonon scattering is the limiting mechanism for the mobility above 200 K. The interesting feature is that below 200 K, the mobility tends to saturate, so revealing the onset of alternative limiting mechanism. Remote Coulomb scattering, induced by intrinsic HfO$_2$ charges, can explain, as for bulk-Si MOSFETs, the mobility behavior. This mechanism may be complemented.
with additional surface and sidewall scattering. In the narrow device, the saturation occurs earlier and the saturation value is less. This is presumably due to the surface scattering on the sidewalls. As the width decreases, the scattering on the sidewalls becomes more important in proportion and the mobility reduces.

At 300 K, the drain current leakage (Fig. 15) is the same order of magnitude than the gate current (2 \times 10^{-13} \text{A/\mu m}^2). For high temperature, it is stronger but not enough to be completely de-correlated from the gate current. This is why the classical activation energy (E_a/2) of the leakage current could not be reached.

All above results can be used to explain the temperature dependence of the transconductance and the drain current curves. The current increase with decreasing temperature is a result of the balance between the threshold voltage increase that lowers the current and the mobility increase that increases the current. As a matter of fact, the current gain at low temperature is smaller than the transconductance peak increase, which is only correlated with the mobility.

**Back gate**

The high temperature back-gate measurements show similar trends with the front-gate. The threshold voltage linearly decreases as temperature rises from 300 to 475 K. The
swing is good indicating a very low back-interface traps density. It linearly decreases with decreasing temperature (Fig. 16).

The low field mobility (= 450 cm²/Vs at 300 K) varies in proportion to $T^{-1.7}$ which again is very close to the classical $T^{-1.5}$ law for phonon scattering (Figure 17). The remarkable advantage of SOI MOSFETs is that they offer an in-situ comparison of the HfO₂-Si (front channel) and SiO₂-Si (back channel) systems. Both interfaces show a low density of traps. However, the mobility is far better at the back channel which suggests that specific defects do exist in the high-k dielectric and trigger additional scattering mechanisms.

![Figure 16](image1.png)

**Figure 16.** Back threshold voltage and swing versus temperature (SOI MOSFETs).

![Figure 17](image2.png)

**Figure 17.** Low-field mobility at the back channel for high temperature.

Conclusions

We have presented low temperature measurements of the effective mobility which consistently show that HfO₂ MOSFETs exhibit more Coulomb scattering than SiO₂ devices. The Coulomb scattering, responsible for mobility degradation, has been further investigated using CVS stress. A correlation between the trapped charges and the mobility behavior has been proposed, which could explain the lower mobility degradation observed in HfO₂ p-MOSFETs. Low and high temperature measurements on advanced fully depleted SOI devices with mid-gap metal gate and high-k gate oxide dielectrics show similar qualitative trends. The drain current, transconductance, swing and low-field mobility are all greatly improved by low temperature operation. However, below 50 K, the device performance tends to saturate or slowly degrades. Even at high temperature (300-500 K), SOI MOSFETs behave better than bulk-Si transistors: the threshold voltage variation is small, the subthreshold swing is nearly ideal, and the leakage current remains reasonable. Since these devices were not optimized for such extreme conditions, we can assume that even better results can be obtained with more specific design. Our results indicate that FD MOSFETs with high-k dielectric and mid-gap metal gate are well adapted to both low and high temperature operation.

Acknowledgements. Thanks are due to our colleagues from LETI, Motorola, CPMA, and STMicroelectronics for device processing, technical support, and scientific advice.
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ROOM-TEMPERATURE SYNTHESIS AND CHARACTERIZATION OF PURE AND Co-DOPED ZnO

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ABSTRACT

A sol-gel method is described for the preparation of powder ZnO and 10% Co/ZnO at room temperature. X-ray diffraction and Raman spectroscopy of the synthesized samples show single phase ZnO structure. Magnetic studies of the as prepared 10% Co/ZnO sample show it to be paramagnetic. However, hydrogenating the sample at 573 K for 6 hrs. changes the sample to a room temperature ferromagnet.

INTRODUCTION

Zinc oxide finds use in a wide range of applications such as catalysis, optical materials, functional devices, cosmetics and UV-absorbers (1-3). Recently, there has been a great deal of interest in Co-doped ZnO for possible applications in spintronics (4-11). Consequently, synthesis of such materials is important for a wide array of electronics and optical device applications which involve fundamental aspects of science and technology. A number of methods, such as sputtering, chemical vapor deposition, sol-gel are commonly employed. In most of these methods, the nature of the produced material is amorphous and an additional high-temperature processing step is required in order to obtain crystallinity. However, high temperature processes can lead to significant constraints, the formation of other phases together with substantial costs for manufacturing. Recently, mechanochemical processing has also been applied for the synthesis of a wide range of nanoparticulate materials involving activation of solid-state displacement reaction at low temperatures in a ball mill (12). Here, we describe a simple room temperature synthesis of pure and cobalt-doped crystalline ZnO nanoparticles by sol-gel method.

EXPERIMENTAL DETAILS

In this process, zinc nitrate or acetate solution was reacted with a base such a NaOH so that the pH of the solution becomes 12. Then, the reaction mixture was left overnight and the precipitate allowed to settle at the bottom. The clear solution was removed and replaced with water and again left for 3-5hrs. This process was repeated four times until the pH of the solution becomes 7. Finally, the precipitate was dispersed in alcohol and dried under vacuum. For cobalt doping, proper amounts of cobalt nitrate for 10% concentration was added to zinc nitrate solution. In the above reaction a zinc hydroxy nitrate complex is first precipitated which slowly transforms into ZnO, NaNO₃ and water according to the following equations.

\[ \text{Zn(NO}_3\text{)}_2 + \text{NaOH} \rightarrow \text{Zn(NO}_3\text{)}\text{(OH)} + \text{NaNO}_3 \quad (1) \]
\[ \text{Zn(NO}_3\text{)}\text{(OH)} + \text{NaOH} \rightarrow \text{ZnO} + \text{NaNO}_3 + \text{H}_2\text{O} \quad (2) \]
The vacuum dried powder was then analyzed by X-ray diffraction (XRD). Figure 1 shows the XRD patterns for pure, 10% Co-doped ZnO and 10% Co-doped ZnO hydrogenated at 573 K for 6 hours. It is evident that the XRD patterns show an excellent match with zincite (PDF 36-1451) without any impurity peaks for the 10% doped Co/ZnO indicating a perfect doping of Co into the ZnO lattice. Similarly, 5% doping of Co in ZnO has been synthesized successfully. Therefore, a perfect doping process of a metal ion into an oxide lattice has been found to occur at room temperature. This opens up new avenues for the synthesis of similar high temperature oxides at room temperature.

Part of the powder samples were used for hydrogenation experiments. The hydrogen reduction set-up consisted of a tubular furnace kept inside a continuously vented hood. The sample, contained in an open glass boat, was placed inside the tubular furnace and H₂ gas was passed over the sample at 573 K with the help of a gas flow control unit. Temperature and magnetic field variations of the magnetization M of these samples were then measured using a commercial SQUID (superconducting quantum interference device) magnetometer.
RESULTS AND DISCUSSION

XRD indicated the diffraction patterns are all comparable to pure ZnO indicating no impurity phases of cobalt or cobalt oxide formation. We have also carried out X-ray Fluorescence (XRF) measurements and found out that the amount of cobalt doped in ZnO was 10.4%. Micro Raman analysis for the pure and Co-doped ZnO is shown in Figure 2. ZnO oxide has four atoms per unit cell resulting in 12 (1A1+1E1+2E2+2B1) optical phonon modes (13, 14). The A1+E1 modes are polar and split into transverse (TO) and longitudinal optical (LO) phonons and both being Raman and infrared active. The E2 modes are only Raman active and the B1 modes are infrared and Raman active (silent modes). Significant differences have been observed for the doped and undoped spectra. Specifically, the 2E2 modes appearing at 101 cm⁻¹ has been downshifted to 97.4 cm⁻¹ and the peak at 437 cm⁻¹ also down shifted for 10% doped Co spectra compared to pure ZnO. Moreover, the intensity of peak at 437 cm⁻¹ is significantly reduced and broadened. These observed features are clearly related to the doped Co and may be used as indications for its incorporation.

![Raman spectra](image)

Figure 2. Raman spectra of the as-prepared sample of ZnO and 10% Co/ZnO

The temperature variation of the magnetic susceptibility $\chi$ for the as-prepared (10% Co doped ZnO) sample (prior to hydrogenation) is shown in Figure 3 where the solid line is fit to the Curie-Weiss law: $\chi = \chi_0 + C/(T + \theta)$. This variation is similar to the one reported for the sample of 10% Co/TiO₂ prepared by spray pyrolysis (15). From the Curie-constant $C = 3.1 \times 10^{-3}$ emu-K/gOe and $C = N\mu^2/3k_B$ (with N being the number of magnetic ions/g, $k_B$ = Boltzmann constant and $\mu$ = magnetic moment), $\mu = 4.465 \mu_B$ for the Co$^{2+}$ ion is obtained. This magnitude of $\mu$ is consistent with the high spin state of Co$^{2+}$, assuming that Co$^{2+}$ substitute for the Zn$^{2+}$. M vs. H behavior.
for the 10% doped ZnO at $T = 300$ K is shown in Figure 4, indicating no hysteretic behavior confirming the existence of paramagnetism.

![Graph](image)

Figure 3. Temperature dependence of the magnetic susceptibility of 10% Co/ZnO. The solid line is fit to the equation shown above.

![Graph](image)

Figure 4. $M$ vs. $H$ of 10% Co/ZnO measured at 5 K. The inset shows the expanded view.
Hydrogenation was carried out for the 10% Co doped ZnO at 573 K, and the sample acquires RTFM. Figure 1 shows the XRD pattern for the sample hydrogenated for 6 hrs. This pattern looks similar to the pure ZnO pattern and indicated no significant impurity peaks for the presence of cobalt and cobalt oxides. From the widths of the XRD lines, the average particle size of the ZnO phase is \( \approx 10(2) \) nm, without any major changes upon hydrogenation. The primary aim of hydrogenation is to induce ferromagnetism, similar to our recently reported studies in Co/TiO\(_2\) system (16), where a controlled transformation of a paramagnetic Co doped TiO\(_2\) into room temperature ferromagnet was observed. \( M \) vs. \( H \) behavior at \( T \) = 300 K for the 6 hrs. hydrogenated 10% Co doped ZnO shown in Figure 5, clearly indicates ferromagnetism. Finally, we measured \( \chi \) vs. \( T \) for the 6 hrs. hydrogenated sample under zero-field-cooled (ZFC) and field-cooled (FC) conditions (Figure 6). The absence of a peak in \( \chi \) for the ZFC cases, which is a signature for the blocking temperature \( T_B \) for Co as reported recently for the thin films of Co/TiO\(_2\) prepared by sputtering\(^9\), provides assurance for the absence of Co nanoparticles in our samples. The reported \( T_B \) values of Co nanoparticles of different sizes are: \( T_B \approx 20 \) K (3 nm), \( T_B \approx 50 \) K (6 nm), \( T_B \approx 100 \) K (8 nm) and \( T_B \approx 260 \) K (11 nm) (17-19).

![Figure 5. \( M \) vs. \( H \) measured at 300 K for the 10% Co/ZnO hydrogenated at 573 K for 6 hours. The inset shows the expanded view.](image-url)
In conclusion, a straightforward method has been demonstrated for the synthesis of both pure and Co-doped zinc oxide at room temperature successfully. XRD and Raman measurements show the formation of single phase compound without any impurity and the magnetic measurements show that the as prepared Co-doped ZnO is paramagnetic. However, hydrogen reduction step at 573 K transforms the magnetic nature from paramagnetic to ferromagnetic. This method may possibly be extended to synthesize other doped high temperature oxides at room temperature. Work is under progress for various doping levels of Co into ZnO which will be reported in the near future.

ACKNOWLEDGEMENTS

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REFERENCES

LOW TEMPERATURE COFIRED CERAMIC (LTCC) BASED ELECTRONIC DEVICES
Processing and Reliability
Current trends in electronics are driving demands to decrease the overall size of circuitry and increase the functionality. A variety of different substrate technologies have been proposed to meet these demands. Low Temperature Cofired Ceramics (LTCC) is one of many technologies that offer the potential to solve this problem. LTCC is a mature and robust technology that is finding widespread adoption in a number of key applications. However, all substrate technologies are continually refined in order to expand the capabilities and therefore expand market adoption.

While LTCC has many advantages, there are many challenges involved in processing future products with ever-decreasing circuit feature sizes. In order to effectively exploit the advantages offered by LTCC and meet these demands, advancements in the state of the art are needed. This paper will discuss in detail the current technology limitations as they pertain to high frequency circuits as well as high density interconnect substrates used for digital systems. The impact of tape instability, printing tolerance, embedded passives, as well as layer-to-layer alignment will be discussed including potential solutions.

INTRODUCTION

In the past ten years the growth in the Low Temperature Cofired Ceramic (LTCC) market has been enormous, to an estimated market of over half a billion dollars. This growth has been largely motivated by the use of this technology in handheld communication devices such as cell phone handsets. In addition, significant potential exists for this technology to play an expanding role in other areas such as high performance computing and high frequency applications. However, the continued growth and expansion of the technology is not without its challenges. These include the need for greater control of shrinkage tolerance and therefore final substrate geometry, requirements for fine line/space and via capabilities, and improved layer-to-layer alignment. Additionally, improved capabilities for embedded passive devices with tighter tolerance and a wider range of values are needed.

This paper will address the current state of the LTCC processing and present its limitations. Potential solutions will be discussed along with the new challenges they present. The topics covered in this paper include tape stability, via technology, printing and embedded passives.

TAPE STABILITY

One of the key challenges in future applications that require very high interconnect densities is the stability of the LTCC tape material itself prior to firing. This stability may be impacted.
through the handling process, as well as through dimensional changes created by variations in humidity and heating processes used to cure the inks and via fill materials. Although LTCC material vendors provide processing guidelines for their product lines, variations exist from manufacturer to manufacturer.

**Tape Shrinkage**

Tape shrinkage has become an accepted part of LTCC processing. Scaling a design to accommodate for the expected shrinkage is a common solution that produces accurate and fully functional packages for current feature sizes. Although scaling has proven to be an effective design technique, as the feature size decreases the tolerance associated with shrinkage becomes a greater concern. On average, product lines have a ± 0.2% variation in the X and Y directions, while the Z can vary as much as 0.5% [1,2]. Scaling up a design can account for shrinkage, but variability in the shrinkage will cause problems in predicting the exact length, width and thickness of the final substrate. This section presents the importance of low tolerance in shrinkage as well as some current and emerging methods to decrease tolerance. Emerging methods have shown tolerances as low as 0.04% [3].

Variability is a large concern for operating at high frequency where a small change in the dielectric thickness can completely change the impedance value. Equation 1, for a microstrip transmission line, and equation 2, for a stripline transmission line, illustrate the relationship that exists between line impedance and substrate thickness [4].

\[
Z_0 = \begin{cases} 
\frac{50}{\sqrt{\varepsilon_r}} \left( \frac{W}{W + 4d} \right) & \text{for } W/d \leq 1 \\
\frac{120\pi}{\sqrt{\varepsilon_r}W/d + 1.393 + 0.667\ln(W/d + 1.444)} & \text{for } W/d \geq 1 
\end{cases}
\]

Eq. 1

In equation 2, \( b \) represents the thickness of the dielectric and \( W_e \) is the width of the conducting strip. For microstrip, equation 1, \( d \) is the dielectric thickness and \( W \) is the conductor width.

Variability in shrinkage exists between different designs and can vary as much as 1% from design to design. This has been attributed to the difference in metal loading, the variations in the usage of different numbers of layers of tape, and different tape thicknesses. One way to overcome this issue is to prepare a sample, or set of samples, substrate(s) for the sole purpose of testing the shrinkage characteristics for that particular design.

Shrinkage will continue to be an important concern facing engineers and manufacturers as the industry pushes for larger and larger panels. Increasing the panel size will allow more circuits to fit on one substrate with the same throughput and decrease the overall amount of unused space. While processing larger LTCC panels is attractive for economic reasons, shrinkage tolerance becomes an even greater concern. For a 6-inch panel, 0.2% shrinkage variation results in 12 mils fired dimensional change. For example, in an automatic production line, a 0201 (0.5mm x 0.25mm) chip device at the extreme edges of this substrate may not be correctly placed on the bonding pads since the actual fired dimensions do not match those loaded in the pick-and-place system.

Two potential solutions for shrinkage variability have emerged in recent years. While both solutions approach the problem in a different manner, these solutions prevent shrinkage in an effort to avoid variability and have achieved success in lowering the tolerance.
Near zero shrink materials are based on tape chemistry that actually constrains the shrinkage in the tape to the Z direction. To compensate for the lack of shrinkage in the X and Y directions, the near zero shrink tape shrinks approximately 32% in the Z direction. This approach has shown a tolerance of 0.04% in the X and Y directions, a remarkable improvement over the 0.2% tolerance of conventional tapes [3].

The second approach to combating tape shrinkage is to use constraining layers. Two separate methods are used in this approach. One method involves processing the constraining layer within the substrate to leave it there upon completion (permanent) and the other method is to use constraining layers on the exterior of the substrate and remove the constrained layers as the final processing step (release). Using these methods, DuPont has shown X-Y shrinkage of 0.12% and Z shrinkage of approximately 40%. The tolerance for these methods is 0.04%.

A drawback to the release constraining tape is that it has to be mechanically removed from the substrate. A common technique used for removal is sandblasting, which may not be desirable for packages with delicate circuitry on the top layer. Permanent constraining layers remain in the substrate and have little impact on the electrical characteristics of the package. Permanent structures require one constraining layer for every 6 equivalent thickness layers and must be placed symmetrically within the substrate. [3].

Although shrinkage variation has posed a challenge to LTCC, solutions currently exist to confront this issue and many promising solutions are emerging. Scaling designs and fabricating a sample shrink substrate are two current methods of reducing error related to shrinkage.

Emerging solutions include near zero shrink and constrained tape, which offer tolerances lower than current methods.

**Tape Handling**

Microwave engineers have been pushing the LTCC community to progress towards thin tape. Advantages of such a movement include higher density, higher capacitance for embedded passives and more coupling possibilities. Providing a wider range of tape thicknesses in general will offer more flexibility in fabricating a package with the exact design requirements.

The introduction of thin tape to LTCC processing poses a challenge regarding the handling of the tape. Although two methods are currently in place to stabilize tape, thin tapes are more fragile in nature and tend to have a memory. Slightly mishandling a piece of thin tape will have larger implications than an equal amount of mishandling on a thicker piece. This mishandling could lead to dimensional changes and cause other types of deformation. A concern related to all tape thicknesses is their hydrophilic nature. Preconditioning eliminates most of the moisture within the tape prior to processing, but keeping the tape stable during processing will lessen the effect of any swelling that could occur as a result of moisture absorption.

Two techniques are currently in use addressing tape handling throughout the LTCC process. The first method is to process the tape with the plastic film backing in place throughout each step. The second is to frame the tape. Both provide more stability for the tape than processing it alone, but there are factors to consider during particular process steps.

Leaving the plastic film backing in place throughout processing is the simplest option. Most tapes are purchased with the film already attached,
so no preparation with regard to tape handling is required to begin fabrication. Results in the next section will show that the plastic film backing keeps the tape very stable dimensionally throughout processing. The difficulty in removing the plastic film backing without creating a dimensional change prior to lamination is the largest concern with this method. Adhesion between the film backing and the tape is quite strong causing the tape to be deformed as they are peeled apart. Using a vacuum chuck aids in reducing this effect by stabilizing the tape while the backing is removed, but some change still remains. Another concern with this method for thin tape processing is that via paste tends to pull out of the vias with the plastic film backing as opposed to staying in the tape.

Framing tape provides a mechanical support through means of a stable solid such as stainless steel. The plastic film backing is removed prior to punching and the now unsupported tape is attached to the frame using adhesive. This method eliminates some of the concerns pertaining to the dimensional change that occurs in the previous handling technique. The disadvantages of framing exist with the equipment modifications and tape cracking that may occur. One theory is that drying the tape after each process step gradually shrinks the tape prematurely causing it to crack around the edges. More testing is necessary to see if drying at lower temperatures for longer periods of time will satisfy the drying requirements while preventing tape cracking. Equipment modifications are primarily a concern for economic reasons. When framing is chosen as the handling method, it has to be used on every process step through alignment. If a proper framing system is not already in place at a particular facility, framing will be the more costly of the two handling methods. Framing of thin tape has proven very difficult because of the adhesion exhibited by the tape after the plastic backing is removed. This causes excess deformation making framing the inappropriate choice for this use. In some designs, it may be beneficial to prelaminate adjacent layers to save time and/or decrease handling concerns. Framing does not allow for such a process condition.

Tape handling is of great concern especially as the field moves toward offering thin tape options. Framing and plastic film backing methods are two handling techniques to stabilize the tape throughout processing. While both techniques offer advantages, each facility will need to determine which of the weaknesses would have the least effect on their process.

Dimensional Change

Dimensional change in the tape has been mentioned in both preceding sections and is of great concern for aligning the separate tape layers that will comprise the final substrate. This change occurs as a result of the plastic film removal. Framing tape or using a vacuum chuck during backing removal has improved results. Testing has been conducted to evaluate the dimensional change of tape, which results from the removal of the backing. These results show there is a difference in the machine and transverse direction associated with this removal process.

Figure 1 illustrates the variation in predicting the tape deformation that occurs as a result of the backing removal. The machine direction stretches from 1 to 8 mils while the transverse direction contracts from 1 to 8 mils. If these values could be predicted, designers could compensate for this phenomenon in their designs. Framing is one method of eliminating this issue, but it is not always an option. For situations where framing is not possible,
a system to remove the backing with consistent and predictable results is necessary. Techniques to stabilize the tape during the film backing removal, such as the use of a vacuum, would be valuable.

Tape stability is a concern throughout the LTCC process. Figure 2 illustrates dimensional change in the tape associated with via punching both with and without the backing. With the backing, the tape varies only ±1 mil and only in the machine direction. Separating the backing from the tape not only increases the amount of variance but also introduces variation in the transverse direction. The best results showed a 2-mil change in dimension and 5-mil in the worst case. Again, a method to stabilize tape during the backing removal would make these results more consistent and therefore predictable.

The substrate fabricated in this experiment was also tested after each process step. Figure 3 displays the variance from the starting dimension to the dimension after each step. The tape was processed with the backing until it had to be separated for lamination.

Notice that punching changes the dimension in the machine direction by only 1 mil and that dimension remains constant until the plastic film backing is removed. Removal of the backing introduces transverse dimension changes and a greater difference in the machine direction.

The cause of the dimension change throughout processing when a frame or plastic film backing is not used is attributed to the drying of paste after via filling and printing. Consequences of these changes include printing/via filling misalignment and layer-to-layer misalignment. These consequences lead to failed via connections or to a need for larger catch pads, which is unacceptable in fineline processing.

Although the removal of the plastic film backing currently poses a
problem of dimension changes, the effects of these changes predominantly impact fine-line applications. The use of frames eliminates some of these challenges. Many applications do not need features small enough for these dimensional changes to impact their process. For those applications requiring small features, determining a method to stabilize the tape during removal would make plastic film backed processing more attractive. Even though this data shows the dimensional change, it also displays the great ability the backing has to stabilize the tape throughout processing. This is a great advantage.

VIA TECHNOLOGY
The processing of small vias is a current challenge in LTCC and the demand for their use has increased as the resolution of fine line printing improves. Screen printing had surpassed via technology years ago in terms of the feature size. In order to effectively exploit the advances made in the field of screen printing and fabricate a denser package, the via technology has to achieve equal dimensions. Three main process steps affect the ability for this advancement to occur: via formation, via filling and layer-to-layer alignment.

Via Formation
Via formation occurs using one of three different techniques: chemical etching, laser drilling or mechanical punching. Presently, one could expect a high yield for vias 4-mil in diameter for laser drilling, chemical etching and mechanical punching techniques [5]. Although chemical etching is an option, it is not used in many fabrication facilities because of the introduction of unnecessary chemicals to the process set-up. Four-mil vias are very respectable, but the challenge is to decrease this limit to the 2-mil resolution of advanced screen printing processes.

Laser drilling is capable of small dimensions and can drill with speed and precision. One of the major drawbacks of using this technique is the extra debris introduced to the fabrication facility. The laser essentially burns away the tape where the via should be drilled creating ash. The ash adds to the particle count of the clean room possibly causing contamination later in the process. In addition, because the via is burned, the via wall exhibits a different adhesion chemistry between the tape and the via fill paste.

Mechanical punching is typically used in industry because of the superior quality of vias achieved through its use. The vias tend to have much straighter sidewalls than laser drilled vias, which slope creating trapezoidal shaped vias from a cross-sectional view. Mechanical punching also creates less debris, as the slugs are pulled away with a vacuum for every punch. In general, 4-mil punching is standard and vias as small as 2-mil have been punched in research facilities. The limiting factor in this process seems not to be the process itself, but the limit on the equipment that can be manufactured to produce smaller vias.

Via Filling
Vias may be filled using one of two methods: screen printing or bladder filling. Screen printing is the method commonly used in industry. This process is viewed as a better economic choice because of the large amount of paste required for the bladder fill. As vias decrease in size though, traditional screen printing is not practical. The wire of the screens is simply too large and block the fill to the small vias. The alternative, using this same method, is to print using a stencil [1].

Bladder filling uses air pressure to push the paste through a stencil and into the vias. As previously mentioned, at least 30 grams of paste is needed for
the set up even to complete only one fill. The two challenges for the use of such a set up is obtaining a stencil for small vias (75 micron and less) and aligning the stencil with the tape. Three-mil via filling has been achieved, but further research is necessary to refine the process. In addition to troubleshooting alignment and stencil challenges, pressure and injection time are being investigated in a Design of Experiment (DOE).

Via filling is considered to be the greatest challenge to producing small vias. Although this challenge exists, there are several movements within the field of LTCC that will favor future production of these small vias. The use of thin tape will improve the aspect ratio easing the fill process. In addition, materials besides stainless steel are beginning to make their presence in stencils used in the via fill process. Stencils are now being fabricated through electroforming techniques, using nickel, and have the potential to realize small vias with comparatively thicker resulting stencils than current laser fabrication.

Layer-to-layer Alignment

A common challenge throughout the LTCC industry is alignment of features smaller than 6 mils. While decreasing the size of vias allows researchers to utilize the intricate circuitry possible through printing, if the vias in adjacent layers cannot be aligned, the package simply will not work. Laminating dies have served as the main alignment vehicle for years. This process relies on the use of registration pins and large registration holes in the tape. The use of laminating dies is simple and shown favorable results for vias down to 6-mils. Another solution to alignment challenges is the use of catch pads. Although this addition ensures the electrical functionality of the device, catch pads occupy valuable surface space and decrease performance in high frequency applications. This contradicts the entire purpose of striving for smaller vias in the first place.

A more sophisticated approach to alignment is to use a vision alignment system. With such equipment, industry level manufacturing facilities can achieve less than 10-micron misalignment. Research laboratory setups, similar to the one shown in Figure 4, can achieve less than 50 microns misalignment. Deformation in the tape, as mentioned previously, will have a larger effect on alignment as the via size decreases. If use of a plastic film backing is the chosen stabilization method, the backing has to be removed before aligning. Without the backing to stabilize the tape, there is more room for error while aligning the substrate. Framed tape will not have this problem as long as the alignment equipment is modified for frame use.

Figure 4: Laboratory alignment system.

The end goal of via technology is to form clean, small vias; completely and cleanly fill those vias; and then perfectly align them. Vision alignment systems offer potential for correcting many of these alignment problems. Equipment and processes in this field are
improving, progressing towards meeting the demands of the microelectronics industry. Figure 5 displays some promising results for the alignment of 6 mil vias.

Figure 5: Alignment of 6-mil vias in an LTCC substrate.

PRINTING

Vias supply the connecting technology to link the circuitry created during the printing process. Printing applies the circuitry to the X-Y plane of the tape. Two methods for printing have emerged: screen printing and the use of photoimageable pastes.

Screen Printing

A screen printing machine is used to transfer paste through a patterned mesh screen resulting in the desired pattern on LTCC tape. Similar to the screen printing process for via fill, there is a limitation on the print resolution. Production lines are capable of resolutions as small as 40-micron lines and spaces [6]. Twenty-micron lines and spaces have even been demonstrated, but it was determined to be impractical for large scale production [6].

Although screen printing technology is ahead of via technology in terms of resolution, many challenges are presenting themselves as the industry continues to push for decreasing sizes and increasing capabilities. Eventually the wire diameters and wire counts are going to reach a threshold. Typically higher wire counts are used for fine line printing. A point will be reached where so many wires are squeezed into a screen that they are practically touching, not allowing any paste to be transferred. In addition, the wire diameter is limited by the strength necessary for them to withstand the pressure applied by the squeegee during the printing process.

Edge quality is a large concern for RF engineers. Calculations performed for determining the functionality of a particular circuit are based on exact widths, and if these widths vary the performance significantly decreases. Higher mesh counts and smaller wires are used in fine line printing and diminish some edge quality problems, but scalloped patterns still remain. An example of this problem is a line that is 75 microns plus or minus 10 microns. This is equivalent to an approximately 15% variation in the overall width. Fifteen percent variation is unacceptable for the performance of RF devices.

Successful printing of fine line and spacing design needs careful selection of printing parameters. The recommended parameters include moderate printing speed, soft squeegee, minimum snap-off distance and high squeegee pressure. Using a standard 400 mesh count screen, researchers have fabricated some 3-mil line and spacing designs including spiral/square inductors, transmission lines, filters, and resonators.

Photoimageable Pastes

Although photoimageable pastes have been around for the past 20 years, the full impact of their use has not been exploited until recently. As microwave engineers push for smaller dimensions and tighter tolerances, conventional printing methods do not meet these requirements. While photolithographic processes are common to the field of Integrated Circuit (IC) fabrication, it is
still considered a relatively new process in LTCC. In addition to the conventional LTCC process steps, two more steps are necessary: exposure and development. Figure 6 displays the modified and additional steps necessary for processing photoimageable paste.

![Diagram](Image)

Figure 6: Process for photoimageable pastes.

The photoimageable materials use the inorganic constituents of conventional thick film technology - metal powders, metal oxides, glass powder, and refractory powders - as the backbone of the composition and the source of final fired performance properties. The organic components of PWB photoresist films, polymers, photoinitiators, monomers and stabilizers, are added to these inorganic materials and provide the photolithographic patterning capabilities of the photoimageable materials.

Photoimageable pastes are available as either negative or positive acting. The chemistry of their composition determines whether the paste will experience scission or crosslinking in the areas exposed to UV light. Negative acting (crosslinking) pastes will become less soluble in exposed regions and the unexposed regions will be selectively removed when the tape is developed. Thus, they form negative images of the original artwork pattern. Positive acting (scission) pastes will become more soluble in exposed regions, therefore those regions will be selectively removed in development.

In general, there are many factors that affect the quality of the line resolution in the photoimageable process. There is plenty of information available on the materials and the photoimageable process itself, though little touches on the issue of how different these variables individually affect the process and how variables interact with one another. The etched fineline widths depend on many processing parameters. Extending the exposure time increases the break down of polymer crosslinks, thus producing a more narrowly developed conductor. For example, experiments showed that increasing the exposure time by 5 seconds decreased line widths by 3 microns. It was also found that the highest resolution was achieved when the mask and substrate were put into contact with the aid of a vacuum. During these experiments it was found that etching time was the most important parameter affecting line widths. [7]

In order to achieve optimum operating conditions, it is important that continued research and experiments be conducted to understand more about the variables and their interactions. Parameters of concern for this photoimageable process include:

- Exposure Energy
- Speed
- Pressure
- Temperature
- Concentration
- And Printing Thickness
- Nozzles and Spray Angles
• Nozzle Droplet Sizes
• Time after printing
• Time after developing

EMBEDDED PASSIVES
One advantage of LTCC technology over its counterparts is the potential integration of passive devices, such as resistors, capacitors, inductors, and some RF components into the multi-layer substrate itself. This releases the valuable surface area for reduced board size. However, unlike discrete or surface passive devices, the value of embedded components cannot be adjusted or trimmed to meet the required tolerance, as it is difficult to reach them from the surface.

Resistors
With regard to embedded resistors, the as-fired resistance tolerance is typically 20-30%, but wireless communication - a major current application of LTCC technology - requires 5-10% resistance tolerance. In the NEMI roadmap for integrated passives, the resistance tolerance target is 10%. Researchers employed high voltage pulse trimming or laser trimming through a hole over resistor in an internal layer [8,9]. While 10% tolerance has been achieved in the laboratory, no work was reported in which a less than 10% tolerance have been obtained in volume production [10].

Contributors to resistance tolerance include the resistivity of the ink-material forming the resistor and the geometry of resistor (i.e. length, width, and thickness). Tolerance of length and width vary from 3% to 5%, which are determined by the physical limit of screen printing technology. Nevertheless, thickness tolerance can be as high as 18%. In terms of the tolerance equation that the authors derived, thickness tolerance must be reduced to 8% for a 10% resistance tolerance [10].

In this section, some challenges existing in fabrication of embedded resistors will be addressed, such as printing parameters, resistance uniformity, geometry variation, printing defects, and optimal design.

Printing Parameters. A five-factor and three-level Taguchi design of experiment was conducted to test the effect of printing parameters on print geometry of resistors, including squeegee hardness, squeegee travel speed, squeegee pressure, initial squeegee height, and distance from screen to green tape on the stage (snap-off distance). Except for squeegee pressure, the parameters do not significantly affect print thickness and width of resistor from perspective of statistics. In other words, there must be some other factors contributing to resistance tolerance.

Uniformity of Resistance in a Large Area. In a test vehicle 135 resistors were printed in a 4.5"x4.7" area to test resistance uniformity. Figure 7 illustrates that resistance is not uniform in the fired 3.9"x4.1" area. The variation in the printing direction (from top to bottom) is relatively small, therefore the resistance value is consistent. However, when moving from left to right, the variation increases. On the right extreme of the chart, the variation is much greater than in the center and the left. This may be due to insufficient leveling of the squeegee or the screen during the screen printing process. Clearly, this is an indication that much of the variation in resistor value can be attributed to control of the printing process.
Figure 7: Variation of apparent sheet resistivity.

Further analysis discloses the cause. In Figure 8, negative tolerance or variation means the measured value is less than the average of the statistical sample, and vice versa. In the top chart, the resistors at the most left and right have very high positive resistance variation; and from left to right, the variation changes from negative to positive, which means resistance increases from one edge of the substrate to the other. This phenomenon can be explained from the thickness variation. In the bottom chart, high negative thickness variation occurs at the two extreme ends, which leads to the high positive resistance variation in the top chart. The thickness tends to reduce from left to right. Moreover, wherever the resistance value is low or high, the corresponding thickness is high or low.

Therefore, uniformity of print thickness across printing direction (in columns) is the key for low tolerance. This can be achieved through proper printer setup. First, level the squeegee used for printing parallel to the printer stage, especially the squeegee ends because a couple of mils may be significant in affecting print thickness. Next, adjust the screen frame holding the screen so that the screen is parallel to the leveled squeegee. This adjustment should be confirmed for the whole distance that the squeegee will travel during printing, not only at a certain location. It is vital to make the screen, squeegee, and stage parallel to one another for a uniform print thickness in a large printing area.

Geometry Variation During Printing

During printing, some of the solvents in the resistive ink evaporate and the ink thickens or increases in viscosity. Although the viscosity change during printing cannot be measured, an experienced operator is able to "feel" this change as the time for printing passes. As a result of the viscosity change, geometry of resistor printed on the LTCC green tape varies. Figure 9 shows variation of resistor geometry as the time for printing elapses. In the first several minutes after the ink is applied onto the screen for printing, resistor width is considerably reduced. From seven to seventeen minutes, it is consistent and then decreases again. The resistor length increases before the time reaches seven minutes, and then fluctuates a little bit up to thirty minutes. Thus, there exists a process window for
printing of resistors, in this case the period of seven to seventeen minutes.

![Graph](image1)

Figure 9: Geometry variation versus time elapsed for printing.

**Printing Defects.** As shown in Figure 10, two types of printing defects were detected from various printed samples with different printing parameters. The bump end, Figure 10(a), is a resistor wider at its two ends, and causes a 7.6% width increase as opposed to a perfect printed rectangular resistor. The other printing defect, serrate edge shown in Figure 10 (b), increases the resistor width by 4.25%. They both resulted from inappropriate printing parameters.

![Image](image2)

Figure 10: Typical print defects.

**Optimal Design.** Resistor width and its aspect ratio (ratio of length to width) also have influence on resistance tolerance. In general, (i) resistors smaller than one square have a higher tolerance, (ii) tolerance changes little from 2 squares to 5 squares when the width is over 15 mils, (iii) 20 mil wide resistors with 2 squares to 5 squares have nearly 15% consistent tolerance, and (iv) 5 mil and 10mil width result in high tolerance.

In addition to the size of resistors, the actual sheet resistivity of resistive ink is another concern in design of resistors. Although resistors with different lengths are printed at the same time from the same screen using the ink in the same jar, the longer the resistor, the higher the actual or apparent sheet resistivity (actual resistance divided by aspect ratio of resistor). This means the use of the sheet resistivity value provided by the ink manufacturer for all size resistors will result in shift of actual average values (not tolerance) from desired ones. Accordingly, a preliminary test prior to calculating resistor geometry is necessary to obtain a relationship between apparent sheet resistivity of the resistive ink and aspect ratio of resistors. The apparent sheet resistivity should be used to determine the length and width of resistors in different values.

With the printing process under control and the optimal design discussed above, the resistors in RF performance test vehicles demonstrate less than 10% tolerance as shown in table 1. Although print uniformity and defects contribute to variance in resistance, an understanding of the print process and the paste characteristics can yield similar results.
Table 1: Resistance - actual versus desired.

<table>
<thead>
<tr>
<th>Desired</th>
<th>Measured Value</th>
<th>SH %</th>
<th>Tolerance %</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 cm</td>
<td>24.23</td>
<td>-3.07</td>
<td>7.85</td>
</tr>
<tr>
<td>50</td>
<td>81.49</td>
<td>2.97</td>
<td>7.87</td>
</tr>
<tr>
<td>75</td>
<td>81.44</td>
<td>8.65</td>
<td>6.68</td>
</tr>
<tr>
<td>100</td>
<td>104.28</td>
<td>4.28</td>
<td>9.20</td>
</tr>
</tbody>
</table>

Capacitors

Parallel plate capacitors are the most common form of capacitors found in LTCC substrates. This is due in part to the relatively simplistic design and ease of implementation into the fabrication process. Figure 11 shows a parallel plate capacitor fabricated in LTCC material. Equation 3 provides the simple equation for a parallel plate capacitor. It is important to note that the capacitance depends on the dielectric constant, plate area, and plate distance. All of these factors strongly depend on the properties of the LTCC substrate in which the capacitor is embedded.

![](image)

**Figure 11:** A parallel plate capacitor made using the LTCC process.

\[ C = \varepsilon_r \varepsilon_0 \frac{A}{d} \quad \text{Eq. 3} \]

The dielectric constant, plate area, and plate distance are dependent on LTCC materials and processing guidelines. If the native LTCC tape is used to separate the capacitor plates, then there is a set of dependencies that are present. First, the distance between the plates will be limited by the available thickness of LTCC tape. If a thick tape is used, then the capacitance will be small; however, if a thin tape is used, processing may become an issue. Also, this distance is defined by the Z shrinkage of the LTCC tape, which as previously mentioned may vary. The next dependency involves the area of the plates. To achieve a high capacitance value, a large area is needed, but area is an expensive commodity. The plate area depends on the LTCC tape and its X-Y shrinkage. If the shrinkage varies, then the desired and actual plate areas will not match. Finally, the dielectric constant relies on the material properties of the LTCC tape. Controlling the firing profile of the green tape is critical for achieving the appropriate material values. If the device fires improperly, the dielectric constant may vary beyond tolerances.

There are alternatives to using the native LTCC tape as the separation material between the plates of the capacitors. High dielectric constant (or high K) pastes or tapes may be inserted between the plates of the capacitors. This provides flexibility with all three factors in the capacitance equation. Like the native tape, this creates a new set of dependencies. The distance may be dramatically reduced since the pastes and tapes have thicknesses on the order of microns to a few mils. The dielectric constant is typically in the range of 10 to 2500 for the pastes or tapes while the native LTCC tape is typically in the range of 5 to 10. However, processing concerns arise from the introduction of the high dielectric constant pastes or tapes. The most common problem is that these materials do not match the properties of LTCC tapes, especially during firing. This affects the shrinkage of the ceramic substrate and may cause delamination or camber. To counteract this, researchers try balancing the
material throughout the substrate, but this limits the overall layout of circuits or components.

**Inductors**

Embedded inductors, as well as surface inductors, are normally present as planar spirals of some particular geometry. An example is shown in Figure 12. This type of inductor is relatively easy to fabricate but the design is complicated. Unlike the capacitors, the inductors may only use one layer of LTCC tape for their fabrication. This allows a minimization of used space in the Z direction but at the expense of increased area in the X-Y plane.

![Spiral inductor made from LTCC tape.](image)

Tape shrinkage and print capabilities are the major limiting factors of the inductors. The geometry of the inductor dictates its performance in terms of inductance, self-resonant frequency and quality factor. Several factors affect the performance including the metal line widths, space widths, number of turns, and type of spiral. These factors are influenced by the X and Y shrinkage of the LTCC tape. If the shrinkage is not uniform, then the desired spiral shape will not be produced. The shrinkage impacts the space widths in particular. For example, one axis may elongate and thereby increase the space width, while the opposite is true for the other axis.

Print capabilities limit the inductors in a couple of ways. First, the print quality has a direct impact on the characteristics of the metal lines that compose the inductor. This typically increases the resistance of the line and thereby reduces the quality factor. Second, the minimum feature size of the printing method determines the correlation between the overall inductor size and the capable performance. For example, a 5-mil space and trace inductor requires a larger total area than a similar performing 3-mil space and trace inductor. Ideally, a smaller trace and space inductor performs better and takes up a smaller circuit area. Previous paper sections have discussed the issues of screen-printing and photoimageable pastes.

**CONCLUSION**

LTCC offers the opportunity to meet many of the increasing demands in the electronics industry. This technology is continually pushing the envelope to decrease feature sizes and provide more design options to engineers. As current challenges are pursued, possible solutions introduce new challenges.

This paper reviews the current state and challenges associated with LTCC. These process and material challenges are presented as well as potential solutions. Further research concerning tape stability, via technology, printing and embedded passives will yield even more solutions to these challenges allowing packages to become smaller and more capable.

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NOVEL LTCC FABRICATION TECHNIQUES APPLIED TO A ROLLED MICRO ION MOBILITY SPECTROMETER

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ABSTRACT

LTCC is applicable to a broad range of micro systems. New LTCC techniques for micro-IMS fabrication have improved function, while simplifying the structure for better manufacturability at lower cost, which is critical to widespread implementation of robust sensing capability. A drift tube is fabricated by rolling unfired glass-ceramic tape with thick film features on both sides, including internal electrodes, external connections, seal rings, a buried heater, and an integral precision resistor network. The tube supports itself mechanically through burnout and firing. The assembly of internal components, including an ionizer, apertures, grids, and a target, is accomplished from the tube ends. The high aspect ratio of LIGA grids accomplishes low obstruction with high axial rigidity. Gas plumbing is also incorporated, and a sacrificial material technique which simplifies the exhaust porting is described. Integral transparent windows in LTCC as they may improve a future IMS are also described. Prototypes have detected ion peaks.

INTRODUCTION

This work describes the combination of an unconventional application of existing commercial infrastructure in Low Temperature Co-fired Ceramic (LTCC) technology for microelectronics with LIGA (a German acronym for lithography, electroforming, and molding) to provide improved functionality and simplicity to an ion mobility spectrometer (IMS). A miniaturized IMS that included a large number of stacked elements had been demonstrated previously. Success with the initial model indicated the need for a more producible implementation. It was also recognized, that the same function could be met by a number of other materials and configurations, including other stacked versions. A rolled LTCC tube concept was selected for further development. A fired example of this approach, which eliminates more than 150 parts, is shown in Figure 1.

Figure 1. An LTCC IMS drift tube is rolled, laminated and fired to set shape.
BACKGROUND

Ion Mobility Spectrometer

An ion mobility spectrometer (IMS) is a device which can identify and quantify compounds by ionizing them and transporting them down a drift tube with an electrostatic potential gradient as the driving force. A counter flow of a carrier gas results in collisions that increase the time of flight to a biased target. A potential well is established in the drift section to trap negative ions. When the well is released, the ions travel toward the detector at a speed that is determined by the ion’s mobility. The mobility is a complex function of the mass, shape, and other properties of the ion. The time of flight to the target is measured using a sensitive amplifier and used to determine the species of the ion. The mobility is determined from the time of flight via the equations below where $v_i$ is the speed of the ion, $\phi$ is the potential, $\kappa$ is the mobility, $L$ is the length of the drift region, $E$ is the electric field, and $t$ is the time of flight for the center of the peak.

$$v_i = \kappa E = -k\nabla \phi$$  \hspace{1cm} (1)

$$\kappa = \frac{L}{\nabla \phi} = \frac{L}{t \frac{d\phi}{dx}}$$  \hspace{1cm} (2)

$$\kappa \approx \frac{L \Delta x}{t \Delta \phi}$$  \hspace{1cm} (3)

Figure 2a. shows the location of the ionizing chamber with respect to the

Figure 2. Schematic of operation of micro-IMS stacked version.
apertures, gate, and target in a schematic cross section of the IMS. Figure 2b. shows the gradient with the potential well in place and schematically illustrates the trapped ions for 3 species of compounds also represented in the earlier sketch in Figure 2a. Figure 2c. shows the gradient with the well released, and suggests that the three ionic species travel the length of the drift tube and strike the target with a time distribution that is characteristic of each species. Figure 3 shows what a plot of the output would look like, with species 3 the first to arrive, followed by the others. The output is shown both as-detected and smoothed by averaging. Sharper peaks are desirable because more compounds can be resolved. Effects that would broaden peaks would obscure neighboring peaks. Statistics of collisions suggest additional practical considerations for the time of flight, including tube geometry, temperature, flow rates and triggering.

A perspective view of the baseline micro-IMS drift tube, consisting of a series of stacked metal and insulator plates, is illustrated in Figure 4. Electrical connections were made by spot-welded leads to the appropriate plates. In the baseline design, the grid consisted of a lattice of fine wires. Additional detail in the end-blocks at the front and tail end of the IMS facilitated plumbing of carrier gas, sample gas, and exhaust from the IMS. A separate heater was wrapped around the IMS and this assembly was then thermally insulated. The baseline IMS was assembled in a simple fixture by adhesively joining the

Figure 3. Diagram of raw and smoothed output from three species in IMS.

Figure 4. Stacked micro-IMS.
many plates together to form the drift tube. End-block assemblies were also joined to the drift tube with adhesive.

**IMS Features/Requirements**

**Inertness.** For implementation of an IMS detector, it is desirable to have a chemically inert internal surface with minimum porosity to reduce trapping of contaminates in the tube. The ceramic in the rolled tube is a good replacement for the inert insulating plates in the stacked version. The gold conductors are also inert compared to the edges of the conductive nickel plates. Polymeric adhesive joints between nickel and sapphire plates can provide trapping sites, leaks and can contribute contaminates to the drift tube in reactions with species that are present—not the least of which are chlorine ions.

**Hermeticity.** One of the major improvements that could be made to the IMS tube was to close leaks. Presently, the device is primarily operated as a positive pressure device. Because sample volumes can be small, the flow must be contained. In a negative pressure device, the same benefits would ensue.

**Precision Voltage Divider.** The IMS relies on a voltage divider consisting of a main and reference chain to establish and release the potential well at the drift tube gate. In laboratory models of the stacked tube, discrete precision resistors were matched so that corresponding resistors varied less than 1%.

**Heater.** The IMS is operated at an elevated temperature near 100°C. A capability to increase the temperature even more, for the purpose of desorption and purging of compounds, is a useful consideration for the instrument.

**Ionizer.** Presently, the IMS uses a radioactive ionizer. The baseline used a number of discrete buttons coated with americium 241. The rolled design uses a coated metal strip which is coiled into a ring and spring loaded outward to hold itself in place. The ionizer must not have a line of site view to the outside world to prevent external radiation. The baseline design had right angle flow ports that aided this requirement.

**Biased Exhaust.** When the IMS operates in a selectable polarity, it is desirable to bias the ions of the opposite polarity to the exhaust ports to assist their exit from the device. This is also accomplished with internal electrodes in the end-piece.

**Low-Temperature Co-fired Ceramic**

An opportunity was seen to simplify the construction of the drift tube, improve performance, and include the end block functionality in a single monolithic structure. LTCC was attractive because it is an established technology with a considerable infrastructure and several commercial vendors—both for materials and for fabrication. Others are also developing new applications of LTCC to devices in general and an IMS in particular. Because the thick films are tailored to the necessary attributes, one may select the most inert metallization for internal electrodes, high-conductivity metallization for buried signal lines, a metal for suitable resistor terminations, and more resistive internal metallization for a heater. One could select a product for solder leach resistance or for brazing, and could tailor material loading that
affects the subtle differences in the geometry of the tube. The conventional use of this system involves an organic binder burnout followed by an elevated temperature firing cycle—both in air. We have primarily used a cycle involving burnout at 450°C and subsequent firing at 850°C. We have adjusted ramp rates as required by various details of geometry and material loading.

Commercial tape and pastes were used. Because a rolled design is a unique case, where the inside of the unfired sheet is rolled onto the external surface of the layer below, it is possible to achieve interconnection between the two sides without vias. A nominal overlap distance for electrode lines suffices for this inside-to-outside connection. The lines facing inward on the inside of the tube are capable of setting up an electrostatic field equivalent to the conductive plate edge in the prior design. Areas where solder connections were to be made to prototypes received an additional printed thickness. Because thick film technology has had stable resistor infrastructure for many years, the resistors previously used on the printed circuit board were combined on the tape and even rolled onto the shape of the tube for co-firing. The detail of precision laser trimming was a minor inconvenience for which special fixtures were considered but are not yet needed. Internal structures were inserted into the rolled design with relative ease. Initial success with assembly of a micro-ion mobility spectrometer has been described elsewhere.1,2

We first demonstrated a small diameter micro IMS and are progressing well to scaling it to a larger diameter and length drift tube, since the larger diameter is thought to be beneficial to improve resolution.7 There are only minor technical considerations in scaling up the IMS. The change to the larger design was a design change that provided an opportunity to incorporate additional functionality into the device. As such, the process description will include some steps from each type of prototype. The large diameter tube was shown in Figure 1, and the earlier tube is shown in Figure 5b in comparison to the stacked version it replaces, shown in Figure 5a.

The IMS shown in Figure 5b has been used to resolve actual ion peaks. Figure 6 shows an actual output plot showing the capability to detect both a reactive ion peak (CI") from the carrier gas and an analyte peak including the species trinitrotoluene (TNT).

Figure 5. a) Baseline micro-IMS on printed circuit board. B) Rolled design demonstrated in 6 mm internal diameter shown for comparison.
CONSTRUCTION DETAILS

Printing

Prototype models used conventional thick film screen printing. Additional work using an in-house direct write system and commercial capability (Ohmcraft, Inc.) will also be discussed. To preserve pliability of the unfired sheet, the thick film drying temperature was reduced from 125°C to 75°C. The print layers for the larger tube are shown in Figure 7. At left, the inside electrodes are printed. At center, the outside conductors are shown. Double printed areas are not visible, but improve the durability of soldered areas. The heater insert is a conductive serpentine on a separate tape.

Sizing, Edge Preparation

In preparation for rolling, critical edges, such as the leading edge, are prepared with a taper. Various techniques were used for this operation, including cutting, pressing, and abrasive definition. The latter was most effective in our practice. Without this taper, the underlying layer acts like a shear for the overlying layer during lamination. The structure of the green tape would recover from such an event—and this can be used in making novel parts—but any associated thick films might be irreparably severed. Even with a taper,
or other mechanical discontinuity arising from creative layering, the bend radius needs careful attention when the bend places the dried paste in tension.

**Rolling**

Rolling to date has been performed manually, but in principle is well suited to automation such as even reel-to-reel processing. In early designs, a 6mm diameter tube was constructed in two wraps of 0.25 mm thick unfired tape. In a later design, a total of four wraps was used, incorporating a thick film heater. A cross sectional end cut in a laminated, unfired tube provides the view in Figure 8a, which highlights both the start of the roll and the termination of the roll with the heater layer incorporated at an intermediate level. The overlap area shown is the only joint contact required between inner conductors and outer conductors to bring electrical leads to the exterior. Figure 8b, at the opposite side of the tube, shows the technique for starting and terminating the mechanical incorporation of the heater layer. A taper at the edges prevents the mechanical damage alluded to above. The small dip in the contour of Figure 8b is due to the minor imperfections of the tapered layer overlap.

Conductor mechanical behavior needed special consideration. Because the internal electrodes were rolled onto a mandrel placing them in compression along their length, the thick film was driven into the tape somewhat during lamination without concern for electrical continuity. Subsequent firing of this material resulted in minor relief on the inside surface of the tube. The exterior unfired thick film lines were placed in tension on the exterior of the tube by the same rolling operation. This resulted in some crazing in the unfired state. This crazing healed satisfactorily for thinner prints with proper practice, but was seen to lead to electrical discontinuity and even cracking for excessively thick prints.

Following rolling, a commercial food wrap was an ideal engineering material when rolled onto the outside of the structure, and served the purpose of restraint to preserve the rolled tape position and alignment. When rolled in sufficient thickness, this material was also very effective as a mechanical buffer during lamination.

The heater layer is included with the thick film heater facing outward. It contacts no IMS electrodes as their path has been transferred to the outside lines. The heater contact pads are accessed through openings in overlying layers as shown in the image of a fired tube in Figure 9. As one might expect from the
earlier view in Figure 8, the internal seam is near perfect in that the electrode alignment is good and no mechanical problems are induced.

The heater is an 18 ohm distributed conductive thick film trace powered by a 12 V battery. Initial operation of the heater has been straightforward. It brings a still-air volume at the center of the tube length and diameter to the operating temperature of 100°C in two minutes. This assembly has been thermally insulated and power cycled between about 40°C and 200°C seventeen times with no apparent ill effects. The heater needs further design optimization to provide the proper thermal profile along the length of the IMS tube under actual flow conditions.

Figure 9. Access to heater terminations is through openings in overlying layers.

Lamination

Again using conventional infrastructure an isostatic press is commonly used to effect the lamination of the unfired tape. These structures were laminated at 68°C and 20.7 Mpa (3000 psi) for variable times around a nominal 10-15 minutes.

The assembly is prepared for lamination using a vacuum bagging technique to prevent contact of the pressurized water with the unfired tape. These bags would tend to pinch seams into the tube during lamination but that is mitigated by the buffer material. Attention to the ends of the mandrel also prevented perforation of the bag under pressure. We have also fabricated other fixtures to be able to use the convenience of vacuum bagging and isostatic pressing for special parts by tapering fixture edges. The laminated IMS structure is removed from the mandrel and has sufficient strength to be handled and mechanically trimmed as necessary.

Burnout and Firing

A variety of different burnout and firing cycles have been employed, depending on particular conditions. Slower ramp rates were beneficial as the wall thickness of the tube design and the loading with additional thick film features were increased. In addition, certain parts were burned out in a separate cycle from the firing cycle for the purposes of study. The burnout conditions and resulting success varied with the selection of materials used and the configuration of the sample and the furnace. Early samples were demonstrated in a belt furnace, but for subsequent samples a box furnace was preferred. This is because the tape is laminated into a structure with sufficient strength to support itself and provide excellent roundness when stood on-end for burnout and firing, as shown in Figure 10. In Figure 10a, the tube has changed color due to the onset of burnout during the ramp to the 450°C burnout dwell. Dark stains near the bottom show that binder burnout, which consists of softening, melting, pyrolysis, and combustion, has commenced. Figure 10b shows the tube during the ramp to the 850°C firing dwell. Figure
10c shows the tube near the end of the firing dwell, still glowing red and having shrunk approximately 12%.

To understand roundness, orthogonal diameter measurements were made at multiple internal and external locations. One diameter was keyed to the external seam for reference, and the other was orthogonal to it. Plotted in Figure 11 are points for a typical tube where the diameter in each direction was compared to the overall mean. It isn't surprising that there is a diameter gradient along the tube. The bottom is in contact with an LTCC setter, and the top is free. The diameter is greatest at the bottom of the tube. The diameter in the center, where the loading is most consistent is within 0.5% of the mean diameter. At the top of the tube, there is no thick film loading, and the minimum diameter is seen. The tubes are processed in a length that permits the removal of both ends after firing—a throw away zone shown by the arrow on the plot. As such, sagging was not a problem, and the roundness of the tubes was more than adequate for operation of the IMS, and sufficient for the logistics of sizing the internal components.

In addition, the length was very predictable. In a sample of 8 of the 6mm diameter tubes, the average length was within 250 μm (0.010 inch) of the designed length of 3.81 cm (1.5 inch).

**Resistor firing and trimming**

Resistors were added to the structure to provide the main and reference chain voltage gradient required for the drift tube. The resistor paste is a commercial product with 1MΩ/square sheet resistance. We elected to use short, wide resistors, which provide a built-in trim structure, because they fit naturally on the tube in the spaces between the centers of the leads. We first used a simple band of resistor material that spanned the length of the tube. Because we are co-firing the resistors, it was preferred to not have them cover the electrodes completely. It was possible to routinely trim these resistors to better than 1% of nominal value—even when as fired resistor tolerances were rather coarse as shown in Figure 12. An index

![Figure 10. Burnout and firing cycle. a) 350°C on ramp up to 450°C burnout dwell. b) 550°C on ramp up to 850°C firing dwell. c) 850°C firing, note shrinkage.](image)

![Figure 11. Roundness evaluation tubes.](image)
was used to compare the difference between each resistor on the main and reference chain, normalized to the mean of all values. Here, the as-fired resistances are plotted for both the early 6mm diameter tube with 50 resistors and the more recent 12.7 cm diameter tube with 80 resistors, if only to show that in both cases the as-fired variance is large. The dark symbols plotted near the zero index for a trimmed tube with 50 resistors show that the trimmed result is more than adequate. This trimming was done both in house and commercially (Ohmcraft, Inc.). Direct writing was also considered in both the co-fired sequence and the post-fired sequence. Trimming of these resistors on a cylindrical surface was performed.

![Graph showing resistance comparison](image-url)

**Figure 12.** Laser trimming of resistors with large variances results index values less than 1%. The index is \( \frac{(R_{\text{main}} - R_{\text{reference}})}{\text{MEAN}} \).

![Images of resistor designs](image-url)

**Figure 13.** a) Trimmed resistors on a round tube. B) Another early resistor design. C) Electrodes and resistors created by the direct-write technique (Ohmcraft, Inc.).
routinely. A design wherein the trim distances are short enough that the curved surface is inconsequential is one approach. Trimmed resistors are shown in Figure 13a, while Figure 13b and Figure 13c show a comparison of printed features and direct-write features, respectively. We are working to improve the precision in hopes of eliminating the laser trim, including printing following firing, direct writing, and other techniques. Under the best of circumstances, we have post-fired resistors with every index value within 12% of the nominal). The key to eliminating trimming is control of the resistor geometry.

We have characterized the thermal coefficient of resistance for these resistors and have seen a 0.5% shift from room temperature to 150°C. As this affects main and reference chain resistors, it is tolerable in the operation of the IMS. When post-fired features are being considered, we have looked at the effect of refiring, which increases resistor values. Additional attention will be required as reliability of resistors is characterized, but presently no overglaze is employed.

**ASSEMBLY**

When fired, the structure is checked for continuity and isolation, and resistors are checked as part of our characterization during development. Geometrical details such as length, roundness, and straightness are also noted. The tube is sized appropriately for next assembly. The internal structures to be placed fall into three categories: The LIGA grids, apertures and target, and the ionizer.

**LIGA grids**

The use of a grid to create a potential well at the leading edge of the drift tube was desirable. Ideally, such a grid would have a very small cross section, especially near the center, and therefore be non-restrictive. In addition, the grid should have rigidity along the axis of the tube in order to minimize vibration sensitivity (microphonic effects) in the axis of the tube. These criteria were solved by the use of LIGA. Several designs were evaluated, and a number of these were built. Figure 14a shows the two main types that were used. A support ring near the perimeter supports the grid structure. At the perimeter of this support ring, several LIGA springs were designed, to assist holding the grids in place. Various techniques were used.

![Figure 14. a) LIGA screens of orthogonal and radial design. b) LIGA screen installed and soldered in place at internal IMS electrode.](image-url)
to alter the stiffness of the springs. At best, a spring loaded installed grid survived a simple impact test, estimated to impart more than 20 g's acceleration, without moving the grid. In addition, flow rates 100 times greater than the designed flows were tested on some of the weaker springs without any negative effect. Nevertheless, LIGA grids for prototypes were tack-soldered for additional strength. An insertion tool consisting of a wire electro-discharge machined support grooves on a mandrel tip, and a coaxial tapered compression feature resulted in simplifying screen insertion to a process taking a few minutes when performed manually.

**Target and Apertures**

The target and apertures were commercially photo-defined from a nickel plated Kovar sheet (Towne Technologies, Inc.). The undercutting at edges was used to provide additional spring force to hold these components in-place as shown in Figure 15. The target is a central plate supported by small tabs at the perimeter. These structures were inserted manually with a simple mandrel. Care was taken not to scratch conductive traces onto the inside of the tube by placing components near their final position and rotating them into position. When so positioned, they were also tacked with solder to the appropriate electrodes.

**Tube Ends**

Tube ends were also fabricated from LTCC material, with appropriate electrodes. Both sleeve designs (primarily small diameter prototypes) and flange designs (primarily large
diameter prototypes) were used in the course of this work. At the target end, the tube end is basically in place to facilitate plumbing of the carrier gas, and as such was relatively simple. The combination of the central target area and the central gas port behind it blocked the line of sight from the opening to the ionizer. A mechanical sample of one prototype design is shown in Figure 16. At the left is the carrier gas inlet, which admits gas which flows around the perimeter of the target and up the tube. Note that in this mechanical sample, the tube ends are significantly smaller than the center, due to an attempt to expand the commercial thick film ink selection, and its unique loading and restraint of the diameter during firing. Also, this picture was taken at a time when blistering due to loading was not completely solved.

At the ionizer end, the tube end was a multipurpose design, which served to support the ionizer, plumb the sample gas to the appropriate drop-off point, and provide an exhaust port. In the smaller diameter design, spiral ports were crafted and cofired into the structure. The spiral prevented the line-of-sight to the ionizer. A sacrificial material technique was used in the larger diameter design as shown in Figure 17 to accomplish the same purposes. Figure 17a is a model of the use of the sacrificial material to form the exhaust ports. Figure 17b shows how the metal strip ionizer will be formed into a ring and placed in the tube end with the

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**Figure 16.** Mechanical sample of large diameter IMS design showing critical components.

**Figure 17.** Tube end incorporating ionizer and sacrificial volume exhaust ports.
ionizer spring-loaded outward. Figure 17c shows a better view of the exhaust ports on a mechanical sample. These exhaust ports have also been demonstrated, by immersing them in water and producing a flow through them. Note that the flow path can be captured, and ported as required.

**Sacrificial materials**

Sacrificial materials were mentioned in conjunction with the fabrication of the ionizer end piece. Sacrificial material techniques have broader value in microfluidic applications associated with the IMS. Previously, techniques have been employed that create cavities and then use uniaxial lamination or fine geometry such that cavities are not caved in. The general technique as well as a discussion of sacrificial material is included in an excellent review. Sacrificial materials have also been described for wick structures in internal volumes of heat spreaders. This is similar to the principle used to fabricate fluidic channels in printed circuit boards. Meso-scale techniques have even been described which rely on etching of sacrificial layers.

A fabrication technique for cavity and channel formation in LTCC has been employed using a sacrificial material that is removed cleanly during the burnout cycle of LTCC fabrication. The sacrificial material is patterned using a variety of approaches, and included during in the stackup during lamination. Here we describe the use of a low molecular weight polymer sheet that can be easily punched or laser cut to provide anchor lines for cavity perimeters, points of attachment, surface texture, and via fill. Our earliest prototypes involved patterns cut with a scissors. Figure 18 shows microfluidic routing that can include side ports on microsystem boards as well as surface ports that can be used in conjunction with soldered annular seals and interconnections.

Several demonstrations have been completed. One is the serpentine manifold shown in Figure 19. Figure 19a shows the channel as designed in sacrificial material. In a thin polymer of low molecular weight, a pattern can be generated as shown in Figure 19b. This piece has support ligaments that were removed prior to lamination. The lamination and firing produces the piece shown in Figure 19c, which was made into part of an in-line bubbler with 73 cm of channel 100 micrometers tall by 1.25mm wide for demonstration at a flow of 1 liter/minute. The structure was capable of supporting pressures of 0.14 Mpa (20psi).

Another demonstration is shown in Figure 20a where orthogonal flow channels have been constructed on two levels. This part was also immersed in water for demonstration, and the images below show operation of channels on left side, both sides, and right side, as desired. This technique can be used to independently address channels in microfluidics system board applications.
Which we have also demonstrated pneumatically while immersed in a fluid. We have fabricated blind cavities, and have addressed microfluidic interconnection ports as small as 300 \( \mu \)m diameter.

**TRANSPARENT WINDOWS**

Earlier success with incorporating transparent windows into LTCC by cofiring\(^2\) has been demonstrated on the IMS as shown in Figure 21.

The interest in such a feature comes from the desire to use photo-ionization as a future replacement for the
Radioactive source. In LTCC package and lid features, these windows have proven hermetic and a sample of 17 parts has survived 100 temperature cycles from -45°C to 155°C, with 5°C/minute ramps and 30 minute dwell times, without any negative effect on hermeticity. Implementation of such a window could take many forms, but one such demonstration is shown in Figure 21.

CONCLUSIONS

LTCC has been used to fabricate prototype micro-IMS devices with an inherent simplicity that reduces the parts count by more than 150, makes them easier to fabricate and ultimately produce in large quantities. The design improves function and makes the device more robust. A sacrificial material technique has proven useful where a microfluidic application required a mildly tortuous path. Additional innovations in transparent windows will extend the usefulness of the micro-IMS.

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Design of Integrated Modules for Wireless and RF Applications using Multi-Mix® Microtechnology and Green Tape™ LTCC Materials

by

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Abstract

This presentation describes the basics of Multi-Mix® and Green Tape™ Low Temperature Cofired Ceramic (LTCC) technologies. The design and performance of a 28 GHz mixer package using a GaAs MMIC and the 943 Green Tape™ LTCC system with embedded capacitance technology is described including the tradeoffs, advantages and compatibility of Multi-Mix® and Green Tape™ technologies. A design approach combining the technologies offers the designer new options to meet the ever-increasing demands of high frequency packaging.

Keywords: Multi-Mix®, Green Tape™, Low Temperature Cofired Ceramic (LTCC), packaging, GaAs, MMIC, mixers

Introduction

High speed digital and high frequency wireless applications are resulting in the emergence of new interconnecting substrate and package materials to meet the demand for higher density, lower power, improved thermal conductivity, stable physical properties, environmental friendliness and lower cost. However, it can be difficult for any one material system to meet all of these demands. Both organic printed wiring and ceramic material solutions offer high-density packaging and interconnection with stable dimensional and electrical properties over a broad frequency range. Integrated passive components and functions in ceramic are in volume production today for wireless/RF and high-speed digital applications.

Multi-Mix® is an organic technology based on etched copper conductors and PTFE composite dielectric layers that are fusion bonded to form homogeneous multilayer structures. The bonded layers may incorporate etched metal film resistors, passive circuit elements, and embedded semiconductor devices as well as LTCC modules. Multilayer, microwave integrated modules formed using this technology can be as small as 0.2 inches square, and multifunction modules as large as 16 x 22 inches.

Green Tape™ LTCC (Low Temperature Cofired Ceramic) is a system consisting of glass ceramic dielectric compositions in a tape format and high conductivity via and conductor metalizations. Passive functions can be embedded using high k dielectric pastes or tape as well as co-fired resistors and inductors. LTCC modules or packages provide a hermetic multilayer interconnection structure with very uniform and stable frequency and temperature dependent properties.

A design approach using these technologies offers the designer new options to meet the demands of high frequency packaging.

Multi-Mix® Technology

Multi-Mix® is an organic technology for the interconnection and packaging of microwave circuits based on etched copper conductors, plated copper interconnections and PTFE/ceramic/glass composite dielectric layers, which are fusion bonded to form homogeneous multilayer structures. The bonded layers may incorporate passive stripline elements (couplers, filters, dividers), embedded passives (resistors, capacitors, inductors), thick metal heat-sink layers, plated-through or filled via holes and vertical matched-impedance structures, and embedded semiconductor devices as well as LTCC modules.

Dielectric Properties

Multi-Mix® Technology can be used to fabricate multilayer circuits in arrays on panels as large as 16 x 22 inches. The dielectric layers are composed of high stability composite materials, containing primarily
PTFE polymer, with glass and ceramic fillers. The PTFE based dielectric layers have thermal-mechanical dimensional stability matched to copper, brass, and aluminum. The dielectrics exhibit low loss, as low as 0.0009 at 10 GHz, with excellent temperature stability and low moisture absorption. The relative dielectric constant is also stable with temperature, ranging in value from 2.2 to 10.2. Layer thickness values range from 0.005 inch (0.127mm) to 0.100 inch (2.54mm).

A key property in the application of LTCC with Multi-Mix® is the low tensile modulus (x-y) of the organic dielectric which allows the expansion of the laminate to be constrained to 6 ppm/°C greatly reducing the stress applied to the solder joints. This provides an excellent TCE match with LTCC for reliable solder attachment.

Conductor Metallization

Dielectric layers are clad with either 0.0007 inch (1.8 microns) or 0.0014 inch (3.6 microns), electrodeposited or rolled annealed copper. The copper thickness can be electroplated to a maximum of 0.005 inches (0.127 mm). Copper conductor line widths and spaces can be etched to a minimum dimension of 0.0020 inch (0.051 mm), within a tolerance of 0.0005 inch (12.7 microns). External plating finish options include tin or nickel for surface-mount applications, and gold for wirebond and ribbon bond applications.

Interconnection Technology

Matched impedance via hole structures create vertical transmission lines through multiple stripline layers, providing maximum use of the module's Z-plane for stacking microwave functions. Plated-through via holes form the signal interconnection between layers, while ground via slots provide a uniform ground reference and isolation for the signal via. This transition is depicted in Figure 1. In addition, edge plating provides shielding and maintains ground plane integrity. Via features such as holes and slots are machined with a minimum diameter of 0.005 inch (0.127mm) and are electroless plated with copper. Electroplating builds the copper thickness on the via walls typically to 0.0007 inch (1.8 microns) with a maximum thickness of 0.003 inch (0.076mm). Via holes may also be filled with DuPont CB100, Polymer Thick Film (PTF) copper paste, planarized, and further plated with copper, nickel and gold to form a smooth surface suitable for die attachment.

Fusion bonding

Multi-Mix® Technology utilizes an isostatic, fusion bonding process to form a homogeneous dielectric medium without the use of adhesive films. Isostatic bonding is performed with a vacuum autoclave, under controlled temperature and pressure, where the PTFE polymer in the composite dielectric material changes state from a solid to a liquid, and back to a solid again. The resulting homogeneous dielectric provides a lower loss tangent than that achievable with adhesive films, and eliminates additional design considerations of a mixed dielectric medium. Fusion bonding also allows for the formation of metal-to-metal contacts connected through the layers, and air cavities contained within the layers. Active and passive devices can be embedded in inner layer cavities or mounted on the surface of the fusion bonded multilayer structure.

Thermal management

Thermal management of heat generated by active devices and RF power is accomplished by means of thick copper vias and thick metal layers. Heat sink layers and thick metal flanges may be directly laminated to the dielectric layers by fusion bonding. Electroplating can build the copper thickness on the via walls to a thickness of 0.003 inch (0.076mm) and arrays of thermal vias may be used to conduct heat to heat sink layers.

Die Attachment

Bare die may be mounted within a layer cavity or directly to the substrate surface that has been planarized, and plated with copper, nickel and gold.
Embedded Passives

Multi-Mix® Technology includes the capability for embedded passive components. Resistors and capacitors can be fabricated in several ways. Metal film resistors may be etched using Omegas-Ply® foil. Typical values from 10 to 200 ohms are achieved with a ±10% tolerance using 25 or 50 ohms per square material. Thick film ceramic resistors and/or capacitor compositions may be screen printed on copper foil in discrete locations using DuPont Inter* Ceramic Embedded Passives (CEP) technology. [1] The foil is fusion bonded to the dielectric substrate layer and etched to create the circuit pattern. Additional layers of dielectric material can be fusion bonded to create a multilayer structure. The resistor materials are based on a nitrogen fired Thick Film system that uses a Lanthanum Boride conductive phase. Resistivities range from 10 Ohms/square to 10k ohms/square with a ±10% as-screened tolerance. Capacitor values ranging in value from 1 to 1000 pF using a material with a dielectric constant of 1000 can be achieved with a tolerance of ± 10%. Development projects are in progress for application of these embedded passive materials with Multi-Mix® Technology.

The LTCC Process

With LTCC technology an unfired (green) tape replaces conventional Thick Film screen printable paste dielectric. The tape is cast from a slurry of the same inorganic components used to formulate a Thick Film composition. A full discussion of LTCC technology may be found in the references. [2,3,4]

A simplified process flow for Green Tape™ LTCC is shown in Figure 2. Each layer of tape is blanked to size, and registration holes punched. Vias are formed in the dielectric tape by punching or drilling. The conductor traces and via fills are screen-printed or photo-defined.

When all layers have been punched, printed, and inspected, the tape layers are registered, laminated and cofired. The cofire process (i.e., dielectric and conductor fired at the same time) involves much fewer firing steps than conventional Thick Film technology.

943 Green Tape™

Low Temperature 943 cofired Green Tape™ is a low loss, lead free glass/ceramic tape with compatible Au, Ag and mixed metal conductors with excellent high frequency properties. [3,4] Typical key properties are:

<table>
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<th>Value</th>
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<tr>
<td>Dielectric Constant</td>
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<tr>
<td>Thermal Conductivity</td>
<td>4.4 W/m-K</td>
</tr>
<tr>
<td>Typical Via Diameter</td>
<td>4 mils</td>
</tr>
<tr>
<td>Typical Line/Space Resolution</td>
<td>4 mils</td>
</tr>
</tbody>
</table>

943 Green Tape™ is currently available in roll or sheet form in unfired (green) thickness’ of 2 mils, 5 mils, and 10 mils.

943 Green Tape™ Conductors

The 943 system offers a number of conductor compositions for interconnection, bonding & attachment and brazing. High conductivity cofired Gold and Silver conductors for signal interconnection and ground planes are available with compatible via fill materials for each metalization as well as mixed metal applications where external Gold and internal Silver compositions are used for cost savings. Solderable compositions and Gold and Aluminum wire bonding compositions are available. A brazing adhesion layer, barrier layer and braze alloy are offered for applications using metal seal rings, heat sinks or metal lids.

The 943 Green Tape™ system continues to evolve with additional conductor, dielectric and process enhancements under development. LTCC materials offer an excellent combination of properties.
especially for high frequency applications where stable, uniform properties over a broad frequency and environmental range are required.

A 28GHz LMDS Mixer Package

The Mixer Module is a 28 to 31 GHz sub-harmonically pumped GaAs MMIC mixer with an integrated LO amplifier in a LTCC Surface Mount Technology (SMT) leadless chip carrier package with coplanar waveguide (CPW) terminals intended for Local Multipoint Distribution Service (LMDS) applications. LMDS is an excellent vehicle for broadband wireless service and packaging the MMIC using LTCC allows for high volume production while not compromising performance, ultimately reducing cost for the end user.

The MMIC mixer die [5] has a nominal size of 52 mils x 38 mils x 4 mils thick with four 4 mil x 4 mil I/O pads. Three of the pads are interconnected with a 3 mil wide ribbon bond for the RF, LO, and IF sections and the fourth pad with a 2 mil wire bond for DC bias. The die is bonded to the package using an Au/Sn eutectic solder preform. A plastic lid sealed with an epoxi preform is used to enclose the die in the package.

The LTCC Package

The leadless chip carrier was designed with the DuPont 943 Green Tape™ LTCC system. The package consists of 14 layers of 943PS and 943C2 Green Tape™ with an overall size of 236 x 236 mils. A plastic lid is recessed so that the module will mount in the "cavity down" configuration. Minimum line width and spaces are 5 mil and 6 mil respectively and 5 mil vias are used for signal interconnects. The signal traces use a Ag/Pt Thick Film composition for wirebondability, vias are Pt/Pd and the ground conductors Ag for the MMIC epoxy die attach.

Package Design Approach

The three tier "cavity down" configuration was chosen to provide the shortest signal lead lengths with an integral multilayer capacitor in the package base. [6] This required the recessed lid as shown in Figure 3. GCPW I/O footprints were chosen for surface mount interconnection and ease of pick-and-place mounting. This style of interface has proven to be a good combination of performance and easy mounting. Visualization of the complete package indicated that there would be four sections from the I/O to the bond shelf. The four sections are 1.) a GCPW transmission line I/O, 2.) a via transition, 3.) a Stipline transmission line, and 4.) a GCPW transmission line. A math model of each section was created in Agilent ADS and each section was cascaded together to create a math model of the interconnection. Each section was optimized in ADS and then 2-D topology layouts were created of each object. The 2-D layouts were then used to build a 3-D model in CST Microwave Office (shown in Figure 4) and Ansoft HFSS for comparison for a full 3-D EM simulation. Figures 5 and 6 show the results from the ADS math solution and the 3-D EM simulation from HFSS for the complete package signal path thru all 4 sections from I/O to the package bond shelf.

Figure 7 compares the CST and HFSS simulation results for two CPW transitions of the type shown in Figure 1 connected with a Stripline. A tolerance study using volume manufacturing tolerances was performed to achieve the shortest possible signal path from the I/O to the die taking into account die tolerances, die attach and wedge bonding tools and lid clearances. An embedded 100pF multilayer capacitor was designed as part of the base layer of the package using 5 layers of 943C2 Green Tape™ (1.7 mils fired thickness) and connected in parallel to the DC bias terminal. A simplified cross section of the package features is shown in Figure 8.

Figure 3: Three tier cavity for lid recess

Figure 4: I/O to Bond Shelf Signal Path

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The basics of Multi-Mix® and Green Tape™ LTCC technologies have been described. The electronic, mechanical and environmental properties offered by combining the technologies provides the designer with new options to meet the demands of high frequency packaging. Fusion bonding provides the capability for internal cavities for bare die or packaged circuits. LTCC packaged circuits allow for pre-testing of embedded functions. The low tensile modulus (x-y) of the organic dielectric allows the expansion of the laminate to be constrained by the package, greatly reducing the stress applied to internal solder joints. This technology combination can be exploited to provide high density, high reliability functional integration. An LTCC package design for a 28 GHz mixer was described and simulation results of key package features has shown excellent high frequency performance. Testing is now in process to demonstrate and verify the functional performance of the module and the design approach.

References


PLATING TO LTCC

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Abstract

The use of LTCC (Low Temperature Cofired Ceramic) continues to expand into environmentally demanding automotive applications. Such applications include engine control modules, transmission control modules, steering and brake modules, and collision avoidance systems. For some of these applications, typical operating temperatures exceed 100°C and the peak operating temperature can reach 300°C, so the thermal cycle requirements of surface mount components becomes severe.

Along with this severe environment, the complexity of the modules has also increased. This means that there are more wire bonds or flip chip sites that have to be made. The yield on these attachment processes has to be extremely high and the bond must be robust in order to make a high-yielding cost-effective module.

Plating to LTCC thick film conductive attachment pads is one way to achieve thermal cycle life, have a friendlier pad for robust wire bonds and flip chip attachment, and reduce cost. The plating process and the conductive composition have to be developed for each LTCC tape that is to be used.

This paper will present:
1. A general plating process and guidelines for plating to LTCC.
2. The development of conductive materials that work with a particular LTCC and survive the plating process.
3. Data on thermal cycle reliability of surface mounted components, wire bonding, and costing information on the benefits of plating.
Background

LTCC substrates can be composed of an infinite number of glass/ceramic combinations. This gives them the flexibility to have many different electrical and physical properties. For example, they can be designed to have low loss at high frequencies, have high or low dielectric constants, have various thermal expansions, and be crystallizing or glassy structures. This makes them extremely adaptable to a wide variety of electrical circuit applications. However, as a group, they typically only have about one half the mechanical strength of ceramics such as alumina.

When thick film conductive materials are applied to the LTCC surface to form bond pads for solder attach or wire bonding, a reaction occurs during firing that can weaken the surface of the LTCC even more. How far the strength is reduced depends on the composition of the conductive. This inherent mechanical weakness aggravated by conductor reactions can cause early thermal cycle failures of soldered surface mount components. The plating process can attack the LTCC and/or the conductive to make this even worse. The design of the plating process and conductors are critical to making a plated LTCC that can survive thermal cycling.

Another issue with LTCC is the wirebondability and the solderability of the bond pads. When the conductive materials are co-fired with the LTCC, the glass in the tape can diffuse through the conductive and arrive on the surface to hinder the solderability or wirebondability. When making products with many wire bonds or solder joints (in the case of flip-chips), a bad bond or joint can have disastrous results on product yield. Customers are requesting 20,000 – 50,000 wire bonds without a miss. Plating over the conductor gives a glass-free surface that makes these yields possible.

To make less expensive LTCC products, it is common practice to use silver thick film conductive circuits in the inner layers and gold thick film circuits on the surface for wirebonding. The transition from silver to gold is usually done at a via. To prevent open circuits that might result from diffusion at the silver/gold interface during firing, a transition via fill material, usually a palladium/silver or platinum/silver, is used. The use of thick film gold and these transition materials adds cost to the LTCC product. Plating can be done to pure silver conductors and thus eliminate the thick film gold and therefore the need for the transition via fills. The result is a more cost-effective part when plating is used.

LTCC Plating Process

Plating to LTCC is done with nickel, palladium, and gold electroless plating technology over a thick film silver conductor that has been screen printed onto the LTCC and fired. For this work, two LTCC tapes and matching silver conductors were used in a clad configuration. The outer layers on which the plateable conductors are located were formed from Heraeus' CT800 LTCC tape. The inner layers of the structure were made with Heraeus' HeraLock® self-constrained (no-shrink) LTCC tape.
Historically, most of the interconnect plating has been designed for alumina substrates since ceramic-based materials have been required to support the high frequency requirements. Alumina parts are typically metallized with thin or thick film nickel, refractory metals, silver, and thick film or plated copper. The high-end packages have 2 mil lines and spaces, and 4-mil flip chip pads. The key demands in plating these packages have been to develop an electroless nickel process that will provide 100% circuit coverage without bridge plating, and to plate electroless gold to thickness (20-40uin) that gives acceptable wire bond yields with 1.0 mil gold wire. Processes have been developed for plating alumina packages that consistently meet these requirements.

In plating LTCC, a third challenge has presented itself. The binding mechanism between the thick film silver and the tape dielectric is susceptible to chemical attack using traditional plating processes. A unique process has been established to eliminate/ minimize this reduction in adhesion so that the benefits of plating (solderability, leach resistance, aged adhesion, repairability, wire bondability) can be realized.

Typically the metallization that is plated up on the thick film conductors is either nickel/gold or nickel/palladium/gold. Figure 1 illustrates the process flow for these two plating processes. Although it sounds more complicated, the nickel/palladium/gold process is proving to be the lower cost process.

The different process steps are described below:

**Cleaning** is required to remove any dirt, fingerprints, tarnish, etc., from the thick film silver surface. If the metallization is not cleaned properly, there could be an adhesion issue between the nickel and the silver.

**Etching/Cleaner Neutralization** is required to neutralize the surface, and detergents or chelators are used in this step to mildly etch the surface to be plated so it will accept the activation or "seed" layer. Various acids can be used for this step.

**Activation.** Electroless nickel will not deposit directly onto thick film silver. The thick film must be activated or seeded. Current technology for activating metallized ceramic is to utilize a palladium seed layer to initiate the plating of nickel onto the silver. Palladium is complexed by hydrochloric acid in solution becoming palladium chloride. Due to the HCl carrier, this chemistry has a very low pH.

**Electroless Nickel Plate** is an autocatalytic process that involves several simultaneous reactions in an aqueous solution that occur without the use of external electrical power. The reaction is accomplished when hydrogen is released by a reducing agent (normally sodium hypophosphite) and oxidized, thus producing a negative charge
on the surface of the part. The charge causes a layer of nickel and phosphorus to form and this continues until the part is removed from the solution. Since the plating process requires no electrical current, the coating produced is a very uniform structure. Typical electroless nickels deposit phosphorus with nickel. The amount of phosphorus ranges from 2-5% (low phosphorus), 6-9% (mid phosphorus) and 10-12% (high phosphorus). Most electroless nickel baths are acidic and composed of nickel sulfate. Alkaline baths are also available and they are composed of nickel sulfamate. A third electroless nickel option is boron nickel. The use of boron (<1%) instead of phosphorus in the deposit creates a very solderable deposit. The disadvantages of boron nickel are that it is about 10 times more expensive than phosphorus nickel and the deposit is very hard and brittle.

**Palladium Plating** is an increasingly important technology for LTCC that is used to facilitate gold wire bonding. Several years ago, the cost of palladium rose to about $1,200 per troy ounce and it was designed out of almost all electronics applications and substituted with gold. Palladium now costs $220 per ounce, compared to $380 per ounce for gold. Some of the other factors driving the use of palladium technology are:

- Availability of electroless palladium chemistry.
- Gold wirebonding can be achieved with 8 to 15μin of palladium, as compared to 20μin minimum required for electroless gold.
- Palladium chemistry is less expensive than electroless gold chemistry.
- Electroless palladium baths can plate up to 4 metal turnovers as compared to one metal turnover for electroless gold.

Palladium plating can be done in a moderate temperature of about 150°F and in a nearly pH-neutral chemistry (7.4), so adhesion of the plated part is maintained. With a plating rate of 1μin per minute, it plates to thickness in 10 minutes as compared to the 30 minutes required for electroless gold.

**Immersion Gold Plating** is a self-limiting process that deposits typically 2-3μin of gold onto nickel. The purpose of immersion gold is to give the nickel extended shelf life as the gold inhibits the passivation process of the nickel. This passivation layer extends the shelf life to approximately 3 months. Immersion gold is also deposited as a base layer for electroless gold. Because electroless gold will only commence plating on gold, the immersion gold is needed as an intermediate step.

**Electroless Gold Plating** is used to plate 20 to 40μin of wirebondable gold. The bath plates at about 0.8μin per minute, so 30 minutes of bath time is required to achieve the required thickness. The chemistry is pH neutral though and operates at a relatively low temperature of 55°C / 132°F, so adhesion is not impacted despite the extended bath time. The chemistry is composed of multiple components and is based on sodium gold sulfite and sulfuric acid. It requires frequent analysis for gold concentration, stabilizer and pH, and the bath will require replacement after one (1) metal turnover. In spite of these challenges, this is still a more cost-effective process than thick film gold but cannot compete in cost with electrolytic gold. The advantage of electroless gold is that it facilitates 1.0 mil gold wire bonding in high-density packages. This step is not used if only solderability, and not wire bonding, is required.
When Heraeus' clad-no-shrink LTCC is run through this unadjusted plating process, the binding mechanism of the conductors to the LTCC will be attacked and will lift off the LTCC with zero force. In working with CTS and Heraeus, a detailed design of experiments was conducted by Spectronics to identify the variables within each process step that affected the adhesion so that the process could be adjusted to eliminate the attack on the binding mechanism. In parallel, Heraeus adjusted their material to accommodate the modified plating process.

In plating LTCC, the process steps had to be adjusted with the following criteria:
- Decrease time to minimum required.
- Decrease temperature to minimum required.
- Use pH neutral chemistry, where feasible.
- Use "mild" acids or alkalines, where feasible.
- Optimize the nickel process parameters of pH, temperature and concentration.

Acid electroless nickel can be made to plate faster by increasing the temperature and increasing the pH. This higher plating rate means less time in the bath and less exposure to the chemistry. Conversely, a higher plating rate also means the hydrogen evolution will occur at a faster rate. This creates a mechanical or scrubbing effect on the thick film metallization. If the pH and temperature are dropped too low, the bath time can be doubled and there is an increased risk of "no plates". It has been found that there is an optimum pH and temperature for minimizing pH impact. The optimized plating process has no detrimental effect on the LTCC and minimal attack on the conductor.

Conductor Development for Electroless Plating on LTCC

The joint development between a LTCC foundry (CTS), a LTCC materials supplier (Heraeus CMD) and a plating house (Spectronics) has developed and is continuing to improve a plated surface for automotive applications. Although the plating process and materials development could be performed sequentially, it is more efficient to develop the plated surface as a team. This is because the performance aspects of the plated part are extremely interdependent. For example, a conductor that works well for one plating application can fail when used in a different process, either because of differences in the plating process or because of differences in the LTCC manufacturing process. Similar observations can be made from the perspective of either the plating processor or the LTCC manufacturing process.

It was decided that a new conductor was needed for this application. The new conductor would need to fire out more densely, and provide more resistance to undercutting that can occur during the plating process. The new conductor would need a significant content of glass to seal the voids that are found when thick film conductors are fired on zero-shrink substrates.

Experiment 1: Silver/Glass Matrix. Development of a new conductor began with a four-cell matrix experiment using two different silver powders and two glass frits. Both material types were selected based on a large difference in the softening or sintering
temperatures of the materials. There is a window of temperature between the end of organic burnout (about 450°C) and the firing peak temperature (about 850°C - 900°C) where the components of the materials used in the LTCC must densify to form the fired structure. If materials are used that begin to sinter before the organic has burned out, then there is a danger of trapping organic material and causing bubbles or other problems later in the firing. If materials densify at a temperature higher than the firing temperature, then the material will have poor mechanical strength.

The four combinations of silver and glass were made into thick film pastes containing about 85% by weight silver and 3% by weight glass; the remaining portion was composed of an organic vehicle system that burns off during firing of the conductor. The conductor pastes were cofired with the LTCC structures and then plated. Testing the adhesion of the plated parts involves soldering wires onto 80 mil square (2mm x 2mm) plated pads and pulling the wires up from the parts. Table I lists the temperature properties of the materials and the adhesion strength of the parts.

The results in Table I show that the best combination of materials included a late sintering silver and an early-sintering glass. The glass type seemed to be the most important effect, as both parts with the early glass had some adhesion, but both parts with the late glass showed no adhesion. An effect of the late glass is that much of the glass remains at the surface of the conductor after firing. A common way of testing for surface is to look at the solderability of the conductor after it has been fired. This test involves dipping the part into molten solder for a few seconds and then estimating how much of the solder pad remains covered by solder. Figures 2 shows the solder pads of the four conductors described above.

Table I: Effect of Glass and Silver Properties on Plated Conductor Adhesion

<table>
<thead>
<tr>
<th>Paste</th>
<th>Silver Sintering Temperature (°C)</th>
<th>Glass Softening Temperature (°C)</th>
<th>Adhesion Strength (lbs.)</th>
<th>Failure Mode (Interface)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>770</td>
<td>870</td>
<td>0</td>
<td>Plating/Conductor</td>
</tr>
<tr>
<td>B</td>
<td>770</td>
<td>560</td>
<td>4.5</td>
<td>Conductor/LTCC</td>
</tr>
<tr>
<td>C</td>
<td>480</td>
<td>870</td>
<td>0</td>
<td>Plating/Conductor</td>
</tr>
<tr>
<td>D</td>
<td>480</td>
<td>560</td>
<td>2.0</td>
<td>Plating/Conductor</td>
</tr>
</tbody>
</table>

A: 0% coverage  B: 95% coverage  C: 0% coverage  D: 50% coverage

Figure 2: Solder coverage of the experimental conductors A-D described in Table I. The A and C solder pads show regions that are not even discolored after dipping into solder indicating a high coverage of glass on the conductor surface. The B pads show high solderability; the D pads show effects of localized glass pooling on the conductor surface.
A correlation was observed between the solderability of the four conductors and the adhesion of the conductors after they have been fired, as shown in Figure 3. This relationship is caused by the relatively poor adhesion of the plating metallization to glass which remains on the surface of the conductors after firing, in contrast to the good adhesion of the plating metallization to the bare silver of the solderable conductors. This relationship should not be taken as a general result, however. One could easily imagine a highly solderable conductor with very poor adhesion before plating, or a conductor surface with a surface covered by isolated pools of glass and silver that would have good plated adhesion despite having poor solderability. The lesson remains, however, that the glass added to the plateable conductor needs to be primarily located in or under the conductor metallization and not remain pooled on the conductor surface after firing.

Experiment 2: Different Low-Temperature Glasses. There are many types of glasses that can have the same softening temperature, but might have very different affects on the adhesion of the plated conductor. Based on the result of the first experiment, it was decided to test other glasses with significantly different chemistries but which were known to perform well in plating applications. In this second experiment, three glass types (referred to as A2, B2, and C2 in the discussion below) were tested, and each glass type was tested at the 2% or 4% by weight level in the conductors. The A2 glass was the same glass that was used in the B & D cells of the first experiment. After the six conductors described above were printed, it was noted that most of the conductors had formed blisters on the surface; the only exception was the conductor containing 2% of the A2 glass. These blemishes were more severe when double-printing the conductors before firing increased the thickness of the conductors, and even the part containing 2% of the A2 glass showed some blemishes under these conditions. The conductors were plated and the plated adhesion was tested as described in the first experiment; the results are shown in Figure 4.

The result from the second experiment suggested that the C2 glass might be a good choice despite the presence of the bubbling seen with the conductor. In particular, it was hoped that as the glass content was reduced, a region would be found where there would be good adhesion and no surface bubbling. The A2 glass was considered to be less desirable because the peak in adhesion

![Figure 3: Plating adhesion plotted versus conductor solderability for the four conductors described in Table I.](image)

![Figure 4: Plated adhesion plotted versus glass content for the six pastes of Experiment 2. The result from Cell B of Experiment 1 is also plotted for comparison (circled data point).](image)
(≈3%) is close in concentration to the level where bubbling is observed (4%). This was especially significant because the double-printed conductor containing 2% of the A2 glass also showed blemishes suggesting that there was no robust window of high adhesion and blemish resistance with the A2 glass.

Experiment 3: Optimizing Content with C2 Glass. The goal of the experiment was to find a formulation with good adhesion and blemish-resistance. A series of conductors were made with C2 glass contents of 1.6%, 0.8%, 0.4%, and 0.2% by weight in TC0302, a silver conductor containing a late-sintering silver powder. After the conductors were made, they were co-fired on the LTCC substrates and the performance of the conductors was evaluated.

A critical aspect of performance is that the conductors be free of the blemishes noted in Experiment 2. Figure 5 shows a picture of conductor features of the paste made with 1.6% glass that shows these blemishes. The severity of these blemishes was quantified by counting the number of blisters occurring on a 2mm square pad. Figure 6 shows a plot of the incidence of these blisters versus glass content. No blisters were observed on the conductors containing 0.4% glass or less.

The solderability of the as-fired conductors was also tested. The solderability of the conductors is shown as a function of the glass content in Figure 7. These results show that for a glass content of 0.8% or higher there is a significant decrease in solderability. Based on the results of the first experiment it would be expected that this would translate to a decrease in plating adhesion.

The initial and aged adhesion of the soldered conductors was also tested. After the parts were soldered, the parts were placed in a 150°C oven for 68 or 168 hours.
During thermal aging, brittle intermetallic compounds form at the interface between the conductor surface and the solder. The formations of these intermetallics stress the interface between the conductor and the dielectric surface causing the adhesion to weaken with time. This test can predict plating performance: pores in the conductor surface that would allow plating solutions to attack the conductor/dielectric interface would also allow solder to reach this interface and dramatically decrease the aged adhesion. Figure 8 shows a plot of the initial and aged adhesion as a function of the glass content. The results show that the addition of a small amount of the C2 glass frit significantly improves the aged adhesion of the conductors, with the adhesion reaching a plateau at about the 0.4% level.

![Figure 8: Soldered adhesion plotted versus glass content.](image)

The improvement in the aged adhesion of the conductors with added glass is shown by the significant change in the failure mechanism of the aged parts relative to the parts tested without aging. Figure 9 shows the solder pads of the pure silver conductor TC0302 after the initial test. The pads show evidence of the ideal failure mechanism (from the standpoint of conductor adhesion): the wires are pulled out of the solder. Figure 10 shows the TC0302 solder pads after the part has been aged. These pads show an undesirable failure mechanism; the conductor pads have pulled away from the LTCC surface. The addition of 0.4% of the C2 glass dramatically alters the failure mechanism of the aged part, as shown in Figure 11. Here the parts show more desirable failure mechanisms; either the wire has pulled out of the solder or a large chunk of the dielectric has been torn out with the conductor pad.

![Figure 9: TC0302 solder pads after initial adhesion test. The wires are pulled out of the solder. The picture indicates where one of the wires had been located prior to the pull.](image)

![Figure 10: TC0302 solder pads after 68 hours of thermal aging. The conductors have pulled away from the surface of the LTCC](image)
Figure 11: Solder pads of TC0302 containing 0.4% of the C2 glass after 68 hours of thermal aging and adhesion test. Unlike the pads shown in Figure 9, these parts show more desirable failure mechanisms; either the wire has pulled out of the solder or a large chunk of the dielectric has been torn out with the conductor pad.

Based on the results of the third experiment, the conductor formulation containing 0.4% of the C2 glass in the TC0302 formulation is being carried forward for plating optimization. This conductor shows a significant improvement in the adhesion relative to the pure silver TC0302 conductor at a glass level significantly below where blemishes were found. Furthermore, this conductor shows the high degree of solderability consistent with a good plating to silver interface.

**Thermal Cycle Test Data**

LTCC substrates were built with typical 0402 size (i.e., 40mils by 20mils) surface mount components using various thick film conductives for the attach pads. The pads were not plated. The components were soldered onto the pads with a tin/lead eutectic solder. Thermal cycle testing was run from -55°C to +125°C for 7,000 cycles; Figure 12 shows the results of this testing.

![Figure 12: Thermal Cycle Test Results](image)

All of the variations tested had no failures through 2,000 cycles and most made it to 7,000 cycles with less than a 15% failure rate. At 7,000 cycles, however, the parts were mechanically exhausted with components being sheared off at only a few grams
force. Figure 13 shows a failed LTCC substrate after the 0402 component has been sheared off; the pad has completely come off and has pulled a divot out of the LTCC.

Figure 13: Failed 0402 Attachment Pad

Figure 14: Cross section showing crack in LTCC after thermal cycling and before 0402 shearing

Figure 14 shows a failure in cross section of a thermally cycled part before the 0402 component has been sheared off. Note the crack occurring in the LTCC. This testing shows that the surface mount parts remain electrically functional even while their mechanical attachment is deteriorating. Instead of monitoring the electrical connection, a better test of the robustness of plated LTCC conductors is the mechanical shear strength of soldered components. The goal of the plated LTCC was to have the least degree of mechanical deterioration over the thermal cycle testing.

Plating a conventional solderable conductor to improve the mechanical performance can have the opposite effect. For example, the solderable conductor developed for this LTCC has a peel strength of 5.4 pounds using a 2mm pad. When the conductive was plated with nickel, the peel strength was reduced to 2.5 pounds. As described above, the plating process and the conductor formulation needs to be optimized to limit this loss of adhesion strength.

As various conductive/plating combinations were tested and additional design of experiments run, the strength of the 0402 component solder attachment to a plated pad has been improved. Table II shows the attachment strength for different conductive compositions. Conductive Y has better initial strength than the non-plated conductive and also improved aged strength. Figure 15 shows the 0402 component soldered to Conductive Y (plated with nickel/palladium/gold) before and after shearing. The shearing causes the LTCC to fail, which indicates the joint has reached the inherent strength of the LTCC.

Figure 15:
A: 0402 Component soldered to nickel/palladium/gold plated pad.
B: Pads after shear test; divots have been pulled from the LTCC.
Table II: 0402 Shear Test Data

<table>
<thead>
<tr>
<th>Conductive Material</th>
<th>Initial Shear (grams)</th>
<th>48 hrs @ 150°C Shear (grams)</th>
<th>250 cycles</th>
<th>500 cycles</th>
<th>1,000 cycles</th>
<th>2,000 cycles</th>
<th>Status</th>
</tr>
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<tbody>
<tr>
<td>Solderable Conductive Not Plated</td>
<td>1570</td>
<td>1391</td>
<td>1256</td>
<td>1122</td>
<td>599</td>
<td>On test</td>
<td></td>
</tr>
<tr>
<td>Plated Conductive X</td>
<td>1553</td>
<td>765</td>
<td>700</td>
<td>572</td>
<td>248</td>
<td>On test</td>
<td></td>
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<tr>
<td>Plated Conductive Y</td>
<td>2101</td>
<td>1460</td>
<td>1317</td>
<td>1217</td>
<td>1020</td>
<td>On test</td>
<td></td>
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<tr>
<td>Plated Conductive Z</td>
<td>1987</td>
<td>1321</td>
<td>1003</td>
<td>972</td>
<td>962</td>
<td>On test</td>
<td></td>
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</table>

Wire Bond Tests. Wirebond performance is another important characteristic of the conductor/plating process. Fine gold wirebonding requires a smooth surface to ensure a reliable process. The nickel/palladium/gold plating does not smooth out the surface, it only follows the surface of the thick film conductive. Figure 16 shows a rough and a smooth conductor in the green state and after plating. The smooth conductor was easily wirebonded with no misses; the rough conductor was difficult to wirebond and caused many misses. Table III contains the wire bond data for the smooth and rough plated conductives and the thick film wire bondable conductive for comparison. The plated parts wire bond easier and age better than the thick film parts. At this writing, the 20,000 wire bond test is scheduled and work is continuing to evaluate heavy aluminum wire bonding.

Figure 16: Surface Finish Comparisons
Table III: Wire Pull Data

<table>
<thead>
<tr>
<th></th>
<th>Initial (grams)</th>
<th>Aged 1 hr @ 300°C (grams)</th>
<th>Bonding Misses</th>
<th>Surface Finish (microns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thick Film</td>
<td>11.1</td>
<td>10.4</td>
<td>None</td>
<td>1.339</td>
</tr>
<tr>
<td>Rough</td>
<td>9.8</td>
<td>10.6</td>
<td>Many</td>
<td>5.344</td>
</tr>
<tr>
<td>Smooth</td>
<td>12.3</td>
<td>15.5</td>
<td>None</td>
<td>1.370</td>
</tr>
</tbody>
</table>

**Cost Comparisons**

To compare the cost between the plating processes and thick film, an equivalent area was used. The processes were specified as follows:

1. Thick Film: Gold screen printed to 22 microns dried film thickness.
3. Nickel/palladium/gold over thick film silver: 50 microinches of nickel, 8 microinches of palladium, and 3 microinches of gold.

Figure 16 illustrates the results by assuming a cost factor of 1.0 for the thick film process. It is clear that plating is more cost-effective than thick film gold and that using nickel/palladium/gold is the lowest cost process.

![Figure 16: Thick Film/Plating Cost Comparison for Equivalent Area](image)

**Summary**

This work describes the optimization of the plating process and conductor formulations for automotive LTCC applications. The plating processes need to be selected to minimize damage to the LTCC materials. The conductors need to have a dense structure to minimize plating solution intrusion and remnant glass on the conductor surface. The resultant plated part is a product that has equivalent or better surface mount thermal cycle reliability, solderability and wirebond performance. The plating process is also more cost effective than a straight thick film product.
High Zr content (Pb,La,Zr,Ti)O₃ (PLZT) ceramics were fabricated using two different processing techniques: (1) the direct write technique of robocasting and (2) conventional powder processing. Robocast PLZT 8/80/20 ceramics had densities equivalent to conventionally processed samples with fired densities greater than 94% of theoretical value after being fired at 1300°C for 6 hours. Both the low field dielectric constant and high field polarization values were essentially the same (within 5%) for the robocast and conventionally processed ceramics. Specifically, dielectric constants measured at 25 °C and 1 kHz were on the order of 2400, while polarization values of 25 µC/cm² were obtained for 50 kV/cm fields at 10 Hz. High temperature dielectric properties were of interest in this study. Extremely low loss behavior (DF < 0.006) and relatively high dielectric constants (K > 3000) were measured over a 100°C temperature range between 60 °C and 160 °C.

I. INTRODUCTION

Development of integrated, volumetrically efficient, high temperature capacitor technologies are desired for a number of power electronics applications. These applications include dc bus capacitors for inverters for electric hybrid and fuel cell vehicles as well as pulse discharge capacitors for missile detonation systems. A key issue is to improve the high temperature dielectric properties of capacitors for both fuel cell vehicle (greater than 140°C operating temperatures compared to the present 85°C) and for aircraft applications (100°C to 300°C operating temperatures). Although initial work on high Zr content PLZT dielectrics was reported 20 to 30 years ago, there has been a renewed interest in these materials due to extended temperature regions of relatively linear dielectric behavior and high electrical breakdown strengths that can exceed 150 kV/cm. The high energy density PLZT dielectrics that exhibit these properties in our studies contain 70 mol% or more Zr and have La contents that range from 3 to 20 mol%. Haertling and Land presented the first phase diagrams of the PLZT system and demonstrated that dielectric constants greater than 1000 could be achieved for mixed phase regions within the high Zr content region of this system. In related work, Schulze and Biggers demonstrated that very high dielectric constants were achievable using relaxor-like PLZT x / 65 /35 ceramics. While dielectric constants in excess of 10,000 were obtained, these materials did not have the field and temperature stability of the dielectrics in this study. There also has been recent interest in relaxor type PLZT behavior. Viehland and coworkers demonstrated increased relaxor behavior by
altering composition in PLZT x/65/35 materials and related this behavior to changes in
domain configurations. Samara\textsuperscript{9} has demonstrated a pressure induced cross-over from
normal ferroelectric to relaxor (12 kbar) to paraelectric (20 kbar) at 50°C for PLZT
6/65/35 ceramics.

A primary goal of our work is to demonstrate that we can fabricate high energy
density, high Zr content PLZT dielectrics using a materials processing technique that is
compatible with rapid prototyping of integrated ceramic devices. We have chosen the
direct write technique of Robocasting for this study, since we have already
demonstrated\textsuperscript{10} fabrication of high Zr content PZT (PZT 95/5) composites and monoliths
that can withstand fields of 30 kV/cm and hydrostatic pressures greater than 300 MPa. It
is noted that several direct fabrication techniques have recently attracted much interest for
rapid, agile manufacturing and prototyping of ceramics. Examples include fused
deposition of ceramics,\textsuperscript{11} three dimensional printing,\textsuperscript{12} and robocasting.\textsuperscript{13} Robocasting is a
computer controlled slurry deposition technique developed by Cesarano and coworkers\textsuperscript{14}
that deposits highly concentrated colloidal slurries with low organic content (less than 1% by weight) to construct complex 3-dimensional components in a layer-by-layer build
sequence. It is thus highly suitable for the ultimate goal of integrating high energy
density ceramic dielectrics into integrated ceramics packages. The desired slurry
rheology is pseudoplastic with a yield stress, facilitating extrusion through an orifice
(100-800 μm diameter) and forming a continuous cylindrical bead. The rheology of the
suspension used in robocasting must be carefully controlled; it is desirable to have a high
solids loading (>50 vol. %), as this prevents cracking during drying, and produces high
density green pieces. Additionally, pseudoplastic behavior is also desirable, as this
allows the suspension to flow through an orifice under an applied stress, yet maintain its
shape once deposited. Cesarano and coworkers have demonstrated that feature sizes
smaller than 100 μm can be fabricated using suitable rheological control.\textsuperscript{13} We
demonstrate in this report that high temperature, high energy density robocast dielectrics
can be fabricated with essentially equivalent physical and electrical properties to
conventionally processed ceramics.

II. EXPERIMENTAL PROCEDURE:

Both bulk and robocast samples were prepared from 500 gram PLZT powder batches.
These batches were formed from commercially available oxide powders (PbO\textsuperscript{a}, La\textsubscript{2}O\textsubscript{3}\textsuperscript{b},
ZrO\textsubscript{2}\textsuperscript{a}, TiO\textsubscript{2}\textsuperscript{b}), which were combined in appropriate proportions to achieve a final
La/Zr/Ti stoichiometry of 8/80/20. Batching was calculated assuming that the La
substituted on the A-site and created B-site vacancies. In addition, 2 mol% excess Pb

\textsuperscript{a} Alfa Aesar. Ward Hill, MA

\textsuperscript{b} ACROS. Morris Plains, NJ
was incorporated to improve sintering behavior. The constituent oxides were weighed, placed into a Nalgene jar, and ball milled in ethanol for four hours using ZrO₂ milling media. After milling, the powder was dried and calcined at 750°C for four hours. In order to reduce agglomeration, the calcined powder was milled after calcining for twelve hours in ethanol.

PLZT powder compacts were formed by two different methods: (1) conventional uniaxial pressing and (2) robocasting. Powders for conventional pressing were stored for 24 hours in a plastic container to obtain uniform moisture content. Green body compacts of approximately 1 cm diameter by 1 cm height were formed from approximately three grams of powder. A pressure of 100 MPa (14 ksi) was used to uniaxially compact the powder into green bodies.

Robocasting requires that the PLZT powder be in the form of a flocculated suspension that is on the verge of dilatancy. To produce the desired rheology, 50 grams of calcined PLZT powder was suspended in 18 grams of water, as well as several processing additives. A sodium silicate dispersant (Darvan 821) was used to disperse the powder, while Surfynol was used as an antifoaming agent. Methylcylic was also added to improve rheological properties. These constituents were mixed thoroughly in a Nalgene jar using a paint shaker apparatus. After mixing, PbNO₃ was added in small increments to adjust the pH until the suspension flocculated. The ready-to-cast suspension was then loaded into a syringe, and placed onto the Robocaster. This apparatus consists of a computer controlled, three-axis positionable table onto which a part is cast, as well as a mechanism to hold and dispense the suspension from the syringe at a controlled rate. Similar to stereolithography, parts are built up in layers, with new layers being deposited on top of subsequent layers until an entire part is built. For the samples in this study, individual square layers of dimensions (15 mm x 15 mm x 0.5 mm) were cast using a syringe needle with a diameter of 500 microns. Ten layers were built up until a part of final dimensions (15 mm x 15 mm x 5 mm) was built. These parts were allowed to dry for 24 hours in ambient atmosphere to minimize cracking during firing. Samples were loaded into covered alumina crucibles on setters of similar PLZT composition and surrounded by a PZT 95/5 burial powder to prevent lead loss during firing. The crucibles were placed into a furnace and heated at a rate of 2°C/min up to 1300°C and held for 6 hours before cooling to room temperature at a rate of 3°C/min.

PLZT samples for electrical testing were prepared from both the conventional process and robocast as-fired ceramics using a diamond saw and mechanical polishing. The conventionally processed PLZT test specimens were sliced from the as-fired cylinders into disk shaped samples with a thickness of 0.75 mm and a diameter of approximately 8 mm. The robocast ceramics were machined into rectangular samples having dimensions of approximately 10 mm x 5 mm x 0.75mm. Both samples were prepared for electroding by a 600 grit SiC grinding procedure followed by a 12 µm diamond polish. After machining and polishing, a 20 nm chrome adhesion layer followed by a 150 nm gold electrode layer were sputter deposited onto the samples.
Capacitance and dissipation factor of our PLZT samples were measured using an HP 4842 precision LCR meter at frequencies ranging from 100 Hz to 1 MHz. For dielectric property versus temperature measurements, samples were heated and cooled at a rate of 2°C/min. Temperature and capacitance data were recorded using Labview data acquisition software. Polarization versus electric field data were taken using a Radiant Technologies Precision Material Analyzer. Samples were tested at applied fields of 10, 30, 50, and 75 kV/cm at a frequency of 10 Hz. Dielectric hysteresis data was taken at 25°C, 75°C and 120°C. These three temperature regions represented strong relaxor, weak relaxor and temperature insensitive behavior, respectively.

III. RESULTS AND DISCUSSION

Green and fired densities of both the bulk and robocast samples are given in Table I. It is evident that the green density of the robocast samples is significantly lower than that of the bulk material. This is due to the relatively low solids loading of the flocculated robocast suspension, approximately 43 volume percent. Typically, these suspensions have solids loading of at least 50 vol. %, but due to the diluent behavior of this suspension, it was necessary to lower the solids loading to allow it to flow through the syringe without clogging. It is noted that the present powders have not been optimized for robocasting. Chemical preparation of powders, spray drying and impact milling are among the techniques that would result in a more uniform, nonagglomerated particle size that would permit greater solids loading and thus greater green densities. As a result of the low solids loading, there was cracking observed for some samples when allowed to dry in ambient air. This is most likely due to the large degree of drying shrinkage, and the relatively fast rate at which it occurred. Even though the green densities of the robocast samples were significantly lower, this did not negatively impact their fired densities. In fact, these samples had slightly higher densities than the bulk samples, 96% versus 94% of theoretical. Density gradients due to die-wall friction in the bulk ceramic samples likely contributes to lower fired densities than robocast samples, which are more homogeneous in the green state.

Table I. Density data for both pellets and Robocast samples.

<table>
<thead>
<tr>
<th></th>
<th>Green Density (g/cm³)</th>
<th>% Theoretical</th>
<th>Fired Density (g/cm³)</th>
<th>% Theoretical</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk Ceramic</td>
<td>4.52</td>
<td>54.9</td>
<td>7.39</td>
<td>93.9</td>
</tr>
<tr>
<td>Robocast Ceramic</td>
<td>3.00</td>
<td>37.5</td>
<td>7.56</td>
<td>96.0</td>
</tr>
</tbody>
</table>

The dielectric constant and loss for both the conventionally prepared and robocast samples are shown as a function of frequency in Figure 1. Typical relaxor-type behavior is observed for both sample groups. Dielectric constants in excess of 2300 at 1 kHz were obtained at room temperature. While the average values of the dielectric constant between the two groups differ by approximately 100, the standard deviations are large
enough that it cannot be said that there is any significant difference. Loss at 1 kHz was found to be 0.030 for the bulk samples, and 0.022 for the robocast samples at 1 kHz.

PLZT 8/80/20 ceramics showed a dielectric constant that exceeded 3000 from 60°C to 160°C and a dissipation factor less than 0.007 from 90°C to 180°C as shown in Figure 2. X-ray diffraction data indicates that this region of high dielectric constant and low dissipation factor consists of cubic and rhombohedral phases. As temperature increases, the dissipation factor decreases from 0.02 at 60°C to 0.007 at 90°C where it remains constant until 160°C. The breakdown strength of our material actually increases with temperature from 25°C to 74°C, corresponding to the reduction of the dissipation factor. The factor of two increase in breakdown strength corresponds to roughly a factor of 4 increase in energy density for these PLZT ceramics that exhibit nearly linear field behavior. Only a 16% change in high field (50 kV/cm) polarization from 25°C to 75°C was measured.

X-ray diffraction measurements that were performed from 25°C to 200°C provided an interesting correlation with the dielectric behavior. At 25°C, 30% cubic phase and 70% rhombohedral phase provided the best fit from Rietveld analyses. As temperature increased, the effective amount of rhombohedral phase decreased. Further, as can be seen in Figure 3, the full width half maximum corresponding to different d-spacings decreased as temperature increased, indicating the onset of a more symmetric phase. The (200) peak shows a pronounced decrease in FWHM values for the (200) d-spacings. Rietveld analyses indicated that the low dissipation factor phase contained a higher volume...
fraction of cubic structure. Our work indicates that robocasting is a viable technique for prototyping integrated high energy density dielectric ceramics.

V. FIGURES

Fig 1. Dielectric constant and loss as a function of frequency for both conventionally processed and Robocast PLZT 8/80/20 ceramics.

Fig. 2. Dielectric constant and dissipation factor as a function of temperature for PLZT 8/80/20 robocast ceramic.
Fig 3. FWHM for various XRD peaks as a function of temperature.

Fig 4. Polarization as a function of electric field for conventionally pressed pellets. Data were taken at 10 Hz and at several temperatures: -55°C, 25°C, and 75°C.
Acknowledgments

The authors are grateful to Mike Lanagan, Jim Smay, Jennifer Lewis, John Stuecker and Mike Neihaus for technical discussions. Walter Olson and Jill Wheeler are acknowledged for outstanding technical assistance. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

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15 J. Cesarano III, P. Calvert, "Freeforming Objects with Low-Binder Slurry," U.S. Patent Number 6,027,326
THERMAL MANAGEMENT USING LOW TEMPERATURE COFIRE CERAMIC (LTCC)

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ABSTRACT

With increased power densities for devices, new methods for thermal management from the heat generation at the die to heat removal to the ambient must be addresses. New methods of active cooling, utilizing an integrated approach of phase change thermal transport and fluid cooling integrated at the substrate level have been investigated using low temperature cofire ceramic (LTCC) technology. This required the development of high thermal conductivity thermal vias, integrated micro heat pipes, porous wicks, micro and macro channels and micro heat exchangers for fluid cooling. New materials, including via inks and cofire thick Ag tape, allow the development of hermetic thermal via structure with 80% area coverage of the Ag conductor. Free standing Ag metal columns and foils within cavities have been developed for the micro heat exchanger methods of heat transfer. These developments in LTCC processing allow optimizing the various thermal elements for the maximum heat transfer from a systems approach.

INTRODUCTION

Low temperature co-fire ceramic (LTCC) is finding increased usage as an interconnect substrate, especially in microwave applications due to the high conductivity of the conductors and low loss of the LTCC dielectric (1-2). However, in addition to high systems speeds, power levels demands exceeding 500 W/cm² are projected, which greatly exceeds the limit of convective cooling (around 5 W/cm²). New methods of thermal management, optimizing an integrated approach of convection, conduction, and thermodynamic cycles, must be developed for the higher heat loads of new devices (3). Since thermal management must consider the complete thermal path from heat source to heat sink, the thermal management approach must consider the entire system. To maintain identical junction and ambient thermal resistance, complete integration of the thermal management from the chip through the system will be required, including capabilities equivalent to closed-loop cooled systems.

Research has focused on the integration of thermal management sub-systems integrated into the LTCC substrate, including the development of high density thermal vias, cofired thick Ag tape for lateral heat spreading, embedded micro heat pipes, micro heat exchangers and micro channels. This paper will review each of these developments.
EXPERIMENTAL

DuPont 951, a commercially available, Ag compatible, cofireable green tape was used as the LTCC material in this study, although the processes described are compatible with any LTCC tape. The thermal vias were fabricated by drilling vias in the LTCC using a high-speed micro-drilling/micro-routing system, screen printing Ag via ink into the vias with vacuum assist, and laminating the system together using either an isostatic or uniaxial laminator.

The thick Ag tape was cast using 3 μm silver powders in a polyvinyl butyral (PVB) tape binder system. The slurry was cast using a doctor blade on a siliconized Mylar sheet, with casting speed approximately 60 cm/min. An isostatic pressing was used for lamination. The LTCC and silver sheets were laminated with 3000 psi at 70°C for 10 minutes.

The microrouter was used to route out the cavity spaces in low pressure laminated stacks of green tape on the layers where cavities existed. To minimize sag in cavities, a wax insert was used. The final structure was fired following the manufactures desired profile, with a peak firing temperature of 850°C and an intermediate hold of two hours at 450°C for organic binder burnout.

Charging of the heat pipe structures is critical for the operation of the heat pipe. A fill tube was soldered to the heat pipe at the fill hole. The charging system included a T-branched fill station, with one side of the T connected through a valve to a high vacuum turbopump and the other through a valve to a precision syringe with a known amount of the working fluid (water). The heat pipe is hermetically sealed to the T and evacuated until the pressure at the vacuum port was approximate $10^{-5}$, at which time the vacuum was sealed off and the working fluid introduced into the pipe. Thermal conductivity properties were determined using a Netsch Instruments Microflash 100. Measurements require calibration samples to be tested along with the test specimen for a comparative analysis to be made.

DISCUSSION

Enhanced Thermal Vias

Enhanced thermal via systems are needed to increase in-plane as well as thru-plane transport of heat in the substrate. The determination of the thermal conductivity, specific heat, and thermal diffusivity for a variety of LTCC systems was performed (4), with ranges for the LTCC and Ag metallizations ranging from 2-4.6 and 217 to 291 W/m-°K, respectfully. Of interest are the properties of via fill ink materials, which have thermal conductivities near 300 W/m-K, approaching ¾ of the value of pure silver, 417 W/m-°K. This difference is probably due to the effect of fine grain size in the unloaded thermal vias. Commercially available LTCC tape materials tested were DuPont 951 and 943, Ferro A6, Heraeus CT700, 800 and CT2000. The Ag data was obtained for via inks for these LTCC systems.
To insure lateral spreading of heat, a thick cofired Ag tape system has been developed [5]. This tape layer, when fired in a sandwich structure that is balanced between the thick Ag tape and LTCC layers, can be fired at any desired thickness, although the tape is fabricated in a nominal 10 mil thickness. The tape material also provides some internal stress relief during sintering which allows for thermal via arrays to be successfully fabricated with via diameters up to 1.1 mm (40 mils) with a spacing (pitch) as small as 1.3 mm (50 mils). Such via systems have via area ratios over 80%, which is over three times higher than typical via arrays using current manufacturer design guidelines. A typical array, with two Ag tape layers, is given in figure 1. The thermal vias are 1mm (40 mils) on a 1.25 mm (50 mil) pitch.

![Figure 1- Enhanced Thermal Vias](image)

To consider the effect of spreading, finite element analysis was performed on a very high power density application. Wide band gap (such as GaN) amplifiers for RF applications have die sizes of 4 mm² with power levels of 25 W. This translates to a concentrated heat source with a heat flux into the substrate of 625 W/cm². A quarter model has been used in this analysis with 4-noded linear tetrahedron heat transfer elements used in ABACUS. Analysis demonstrated [6] that the thru plane conduction is so high that there is minimal spreading, regardless of the thickness of the Ag spreading layer, as shown in figure 2. To optimize the balance between lateral spreading and thru-plane thermal impedance, the via diameter was varied to increase the thermal impedance under the die (increasing the thru-plane impedance), forcing the heat to flow outwards thru the thick Ag planes, enhancing thermal spreading, as shown in figure 3.

![Figure 2 - High Thermal Via with Minimum Spreading](image)
Heat Pipe Fabrication

A heat pipe consists of a sealed hermetic enclosure, with three distinct regions: an evaporator, a condenser, and an adiabatic region separating these two regions. The enclosure contains a working fluid, typically water, which absorbs heat by evaporation at the evaporator, travels as a vapor in the adiabatic region to the condenser, where it condenses and the heat is removed. The working fluid returns to the evaporator section from the condenser by the capillary action of a wick structure.

In the traditional application of a heat pipe, the primary transport of heat is along the axial direction of the heat pipe, essentially from one end to the other, which is shown schematically in Figure 4.

The main body of the heat pipe acts as the adiabatic region separating the evaporator and condenser. This method of heat transport uses the heat pipe to move heat over relatively long linear distances with almost negligible temperature variation along the length of the heat pipe.
In a variation termed a heat spreader, shown schematically in figure 5, the side opposite the evaporator region is a broad condenser region, so that only the surface and sides serve as adiabatic regions. The heat spreader operates by effectively spreading the heat from a concentrated source to a large area where the effective thermal density is lowered by the ratio of the evaporator area to condenser area. The return path for the working fluid must account for 3-dimension fluid flow, as the heat source and heat sink are on opposite sides of the heat pipe, requiring a complex wick structure for optimal application. To fabricate a heat pipe, a large area hermetic cavity must be developed, along with a wick structure which can transport the working fluid from the condenser back to the evaporator.

**Cavity Formation.** If the green density of the ceramic is not uniform after lamination, differential shrinkage will occur, resulting in sagging or cracking. Since there exists unsupported material above and below a cavity, non-uniform density will occur during lamination for a cavity. To overcome this, inserts (7) and the use of low-pressure lamination with adhesives (8) have been utilized. Although an insert can be used for thru channels, it cannot work for closed cavity structures found in the heat pipe/spreader structures. Organic inserts were inserted into the cavity. The inserts used covered a wide range of materials, including waxes, thermoplastics, and thermosets. The insert that contains the desired shape is inserted into a rectangular slot of the green structure. During lamination, the viscoelastic properties of the tape (9) allow flow to conform to the shape of the surface of the insert. During firing, the inserts either melted or wicked into the porous ceramic structure or volitized and exited through the hole in the cavity required for filling with the working fluid. This process allowed for a uniform green density to be achieved, with large area cavities to be formed with no sag or camber, as shown in Figure 6.

![Figure 6 - Large Area Cavity in Heat Spreader Structure](image-url)
**Wick Structure.** For a heat pipe or heat spreader (a multi-channel heat pipe where the heat is removed from the bottom of the system) a wick structure is required to transport the working fluid from the condenser to the evaporator area. The wick structure requires a balance between capillary flow and the total flow. Initial wick structures were developed by a grooved structure and then a porous wick developed from sintering a large particle (150 mesh) Ag powder. An optimized wick, which provided twice the capillary flow of the large Ag powder was produced by a porous wick, developed by coating nano-sized particles of Ag on an organic sphere. Upon firing, the Ag particles sintered before the organic sphere melted, resulting in porous spheres of Ag, as shown in Figure 7.

![Figure 7 – Porous Wick for Micro Heat Pipes](image)

The comparison between the heat spreader and a solid ceramic piece has been made in order to indicate the effectiveness of the heat pipes as shown in Fig. 9. Only a small heat power can be applied to the solid ceramic sample and the comparison can be performed at the maximum heat input of the solid samples. It can be seen from these figures that there are much larger temperature differences along the solid bars than the

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heat pipes/spreaders. In fact, the heat spreader was able to operate at power levels approaching 200 W (10), while maintaining the temperature below 100°C.

![Figure 9- Comparison between Heat Spreader and same-sized solid ceramic bar at 16.7 W/cm² input power.](image)

**Micro Heat Exchanger** - Micro heat exchangers were developed and evaluated for device cooling using an embedded fluid cooling channel integrated into the interconnect substrate. Although channels have been developed within substrates for cooling (11), this new approach utilizes a high-density thermal via array through the LTCC, with the vias continuing as freestanding columns in an open channel within the substrate, as shown in Figure 10. This system provides a low thermal resistance path of 0.1 to 0.2 °C/W, from the component to the bulk coolant flow in the channel. Figure 8 demonstrates free standing columns under a high density via array.

![Figure 10- Sample showing free standing LTCC silver columns within an open cavity, radial (top) and standard (bottom) thermal via arrays.](image)

**Micro Channels** - A micro CPL has been demonstrated in silicon based MEMS devices using an LTCC substrate for a fluid reservoir (12), and one could consider integrating the entire system into LTCC to minimize thermal impedances at the interfaces. However, to
make these feasible, micro channels (25-75μm width) must be developed which can be fabricated into the LTCC. To fabricate the large channels required for micro heat pipes, large organic inserts were utilized that burn out upon firing the LTCC. To fabricate micro channels and micro cavities, micro-definable organic films (photoresists / laser definable polyimide) were evaluated to serve as a high precision, fine definition fugitive insert. Kapton was either laser machined or ablated from an attached film bonded to the LTCC. Using this latter method, complex structures could be developed, such as posts (dots of Kapton) which are impossible on a free standing film. Figure 11 is a cross-section of the LTCC showing a micro cavity fabricated by lamination of LTCC over a free-standing laser machined Kapton spacer, approximately 50 μm in width. Notice that there is complete fusion of the individual tape layers without any trace of the junction. Figure 12 represents a large area cavity (1 cm X 1 cm) with micro height (20 μm) fabricated using 25 μm Kapton film. As both free standing and ablated films gave equivalent results, the ability to fabricate complex shaped micro cavities and channels into LTCC is able to be done. Laser ablated films can be used for complex shapes and columns, where the structures cannot be joined or be free-standing.

Figure 11 – 50μm cavity in LTCC using Free standing Kapton insert

Figure 12-large area cavity, 20 μm in height, using large Kapton strip, as shown in Fig. 2

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CONCLUSIONS

1. LTCC offers new methods of thermal management integrated at the closest level of packaging to the heat source, coupled with electrical properties for microwave applications.
2. Integrated heat pipes/spreaders can provide extremely high effective thermal conductivity. When coupled with thermal vias, the overall system thermal impedance is extremely low when compared with any standard interconnect substrate technology.
3. Integration of fluidic cooling systems offers new methods for enhanced thermal management at the component and substrate level.
4. Laser machined Kapton films can be used to develop micro channels and cavities in LTCC. This allows new flexibility into designing devices, using the cavities/channels in novel thermal management devices or as gaps in the dielectric for electrical isolation.

ACKNOWLEDGEMENTS

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THERMOMECHANICAL RELIABILITY OF LTCC SOLDER ATTACHMENTS

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Abstract
Low temperature Cofired Ceramic (LTCC)- based Multilayer Ceramic Integrated Circuits (MCIC) developed within the Microelectronics and Physical Sciences Lab (previously in the Solid State Research Center, SSRC) of Motorola are finding use in many wireless applications due to the advantages of RF function integration, and size reduction. To integrate MCIC applications on a PCB, a variety of solder attachment technologies have been developed over the years. These include ball grid array (BGA), and the MCIC side interconnects for lower profile cellular phone applications. These board-level solder attachments are comprised in dissimilar materials that expand or contract at different rates on various stages of thermal excursions: process cycle and operation cycle. In this paper, the thermomechanical reliability aspect of BGA and side interconnects were examined.

Introduction

The multilayer ceramic fabrication process represents a robust fabrication technology for creating a variety of highly integrated circuit structures useful in the electronic industry. Especially in the wireless industry, the unique RF properties and multilayering enable highly integrated LTCC-based multilayer ceramic integrated circuits (MCIC). Devices demanding many layers (i.e. 10-30) featuring high dielectric and metal Q's and low temperature coefficient of frequency (Tf) – leading to low loss and high levels of RF circuit function integration (1, 2).

MCIC board-level solder attachments are comprised in dissimilar materials that expand at different rates on various stages of thermal excursions. Table I lists the thermo-elastic properties of the related constituents (3, 4). The differential thermal expansion, or mismatch, must be accommodated by the various materials involved. Generally speaking, the systems are subjected to two types of heat exposures: process cycles, which are often high in temperature but few in number; and operation cycles, which are numerous but less in terms of temperature extremes. In this paper, we deal with both, and the reliability issues during the solder reflow process are also addressed.
### Table I Thermoelastic constants (3,4,5,6).

<table>
<thead>
<tr>
<th>Material</th>
<th>CTE (ppm/°C)</th>
<th>Elastic modulus (GPa)</th>
<th>Poisson’s ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dupont 951</td>
<td>5.8</td>
<td>152 (fired)</td>
<td>0.17</td>
</tr>
<tr>
<td>Silver</td>
<td>19.2</td>
<td>72</td>
<td>0.34</td>
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<tr>
<td>10Sn/90Pb</td>
<td>28</td>
<td>21.1</td>
<td>0.4</td>
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<td>96.5Sn/3.5Ag</td>
<td>26</td>
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<tr>
<td>Copper</td>
<td>16.5</td>
<td>117</td>
<td>0.34</td>
</tr>
<tr>
<td>PCB</td>
<td>25 (in plane)</td>
<td>17.23</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td>63 (out of plane)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figures 1 (a) and (b) show the schematic drawings of typical MCIC BGA and interconnect technologies, respectively, which have been developed at Motorola SSRC. The targeted standoff height for the latter is 5 mil (0.13mm). In this work, MCIC BGA reliability was first examined. Two groups of MCIC-BGA with different MCIC surface metals, mixed Ag/Pd and Ag pastes, were examined by SEM after solder reflow and the solder joint reliability was evaluated by mechanical bend tests and thermal accelerated life tests. Coffin-Manson type of reliability curves were constructed with supplementary finite element (FE) analyses. To develop lower profile MCIC side interconnect technology, a parametric study using FE techniques were performed to decide the sample dimensions of candidates for thermal accelerated life tests. Three tests representing different sample processing were conducted. We found that, with reduced MCIC standoff height, the reliability of MCIC side interconnects can still be acceptable.

![Figure 1 Two MCIC solder attachments: (a) BGA and (b) Side interconnects.](image)

**Accelerated Life Tests and Micro-indentation Tests**

All test samples were fabricated with standard LTCC fabrication methods using DuPont 951 tapes and compatible metal pastes.

All the thermal accelerated life tests were performed under -40° to 85°C air-to-air condition with 30 minutes hold at each extreme. The transition time was approximately 20
minutes. Failure for all thermal cycling tests was defined as 10X resistance change. The tests were monitored intermittently. After failure was observed, the cross sections of failed joints were examined by scanning electron microscopy (SEM), optical imaging, X-ray transmission imaging, and a dye penetration technique. The accumulated failure for each test configuration was recorded and the failure distributions were modeled by the Weibull model. The mean cycles to failure for each configuration were calculated.

**BGA interconnects.** The integrity and the reliability of MCIC-BGA interconnects with Ag and mixed Ag/Pd surface metallization pastes were evaluated by thermal accelerated life tests. We used prototype Design 1, with mixed Ag/Pd, and Design 2, with Ag, for thermal tests, and Design 3 (with both metallizations) for mechanical tests (7). All of the solder joints were connected in one daisy chain. SEM was used to check the metallization consumed (scavenged) during the reflow process.

During solder reflow process, most of the silver metallization reacts with the tin in the solder to form Ag₃Sn intermetallic phase, if the silver layer is thin enough. The replacement of silver by the intermetallic phase can create two new interfaces. According to the Hertzian stress field, where the radial stress is inverse proportional to the square of distance from the point of contact. In (8), Vickers micro-indentation technique was developed to investigate the brittle interfacial strength between the intermetallic compound and the solder alloy by varying the loads and the distance between the indentation and the interface.

**Side interconnects.** The test samples, Design 4, had a square footprint of 1.27mm by 1.27mm, with a height of 1.27mm, and 6 I/Os per side in four different configurations on three test runs. Four MCIC configurations (Table 2) were obtained from the parametric study using FE techniques (9), which will be described in the coming section). Note that the standoff height is our constraint for developing a lower standoff height interconnects, and was fixed at 5mil (0.13mm). Each MCIC configuration has three isolated daisy chains.

**Finite Element Analyses**

All the FE analyses were performed using a commercial ANSYS™ software package. The materials were all assumed linearly elastic, except for solder materials when performing thermomechanical analyses. In isothermal micro-indentation analyses, the solder alloy is assumed to be linearly elastic. In this paper, the rate-dependent behavior of 63Sn37Pb and 96.5Sn3.5Ag solders was decoupled from the rate-independent plastic deformation. Note that the mechanical properties of silver/palladium were approximated from those of the silver in the corresponding FE analyses. The material non-linearity is defined by two ANSYS data tables for each solder: one for bilinear kinematic hardening plasticity (Table 3, the numbers were converted from (4)) and the other for the power law creep (Norton),
Table 3 Plastic parameters for bilinear kinematic hardening model (5,6,10).

<table>
<thead>
<tr>
<th>Material</th>
<th>96.5Sn3.5Ag</th>
<th>10Sn90Pb</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Plastic yield strength (MPa)</td>
<td>Tangent moduli (MPa)</td>
</tr>
<tr>
<td>T=-40°C</td>
<td>57.7</td>
<td>118</td>
</tr>
<tr>
<td>T=-10°C</td>
<td>44.9</td>
<td>102</td>
</tr>
<tr>
<td>T=20°C</td>
<td>33.3</td>
<td>70</td>
</tr>
<tr>
<td>T=60°C</td>
<td>23</td>
<td>46</td>
</tr>
<tr>
<td>T=85°C</td>
<td>12.5</td>
<td>18</td>
</tr>
</tbody>
</table>

\[ \varepsilon_{\sigma} = A * \sigma^n * e^{(-\Delta Q / RT)} \]

where \( A, \Delta Q, \) and exponent \( n \) are 1.10X10^{-2}, 94 KJ/mole, and 9.6 for 96.5Sn3.5Ag (10), and 5.63, 66.5 KJ/mole, and 4.25 for 10Sn90Pb, respectively (5,6).

As the preliminary FE results show in (7), the rate-dependent material non-linearity was not significant in this temperature range. For this reason, we applied rate-independent material laws for the rest of the FE simulations. After the preliminary results being verified, analyses were performed for Designs 1 and 2 under board-level thermal life test condition and for Design 1 under the conditions of mechanical tests.

For micro-indentation simulations, surface to surface contact analyses were performed. The Vicker indenter was assumed to be rigid, and was defined as target elements, while the LTCC surface to be indented was defined as contact elements. The indenter tip was defined as the pilot node. Figure 2 shows a typical FE model.

![Figure 2 a FE model for micro-indentation simulations.](image-url)
Results

**BGA interconnects.** SEM images of the cross section of pieces from Design 1 (with Ag/Pd pad) and Design 2 (with Ag pad) after reflow process were shown in Figures 3 and 4, respectively from a parallel study within Motorola by David Richards. In Figure 3, it shows complete reaction of the Ag/Pd metallization with the tin/silver solder after reflow. The arrow in Figure 3 indicates a continuous layer of Ag metal and AgSn intermetallics, as opposed to the weaker dispersed intermetallics observed in Figure 3.

![Figure 3 SEM images of cross section from one of the solder joints of Design 1 with Ag/Pd metallization.](image1)

![Figure 4 SEM images of cross section from one of the solder joints of Design 2 with Ag metallization.](image2)

Displacement-control PCB bending tests were conducted to compare the strength of the solder joints of two MCIC Ag and Ag/Pd surface metallizations with eutectic SnAg solder paste. Results showed BGA's with mixed Ag/Pd can bear only one third of the load of that with Ag. The strength distributions were shown in Figure 5. The strengths of the joints were 37 MPa and 48 MPa using Ag/Pd and Ag, respectively. The latter falls into the published strength of 47 to 53 MPa at higher strain rates (>0.004 s⁻¹) of 93.5Sn3.5Ag solder from
Figure 5 Distribution of the solder joint strength from mechanical bend tests for Design 1 w/ AgPd and Ag metallization

The accumulated failure for each test configuration was recorded and the failure distributions were modeled by the Weibull model. The mean cycles to failure (MCTF) for each configuration were calculated. The results for the Design 2 are comparable with the LTCC chip scale package (CSP) reliability study reported from Unno et al. (11). With the results of the corresponding finite element analyses, the plastic part of the Coffin-Manson reliability curves for Designs 1 and 2, which relates component life and the fatigue parameter (the maximum inelastic strain range), were plotted in Figure 6. It shows that the reliability curves of Designs 1 and Design 2 are significantly different. For the same level of inelastic strain range, the life from the curve of Design 2 is much higher than that of Design 1.

Figure 6 Coffine-Manson reliability curves for MCIC BGA interconnects with two designs.
Figure 7 is the first principal stress contour plot of an indentation test simulation. As we can see, the tensile stress acts perpendicular to the contour circle. The indentation-induced crack at the interface remains essentially along the plane of the interface, rather than following the contour of the maximum Hertzian stress, which could generate "ring"-like crack.

**Figure 7** The first principal stress contour plot of a FE simulation

**Side interconnects.** The results of thermal ALTs and the FE analyses can be correlated and used to construct the plastic part of the Coffin-Manson curve of the three tests for the side interconnects, which are shown in Figure 8. The discrepancies of the curves may be due to the variations in the assembly process. As we expect, the reliability curves for Design 2 of Figure 4 and those of Figure 8 are comparable. The ALT 10% and mean lives for the joints in each of the three daisy chains are shown in Figure 9. Inner joints have expected longer life. This approaches the level of BGA interconnects with a smaller MCIC module and a larger standoff height, if these inner joints are used actively.

**Figure 8** Coffine-Manson reliability curves of three thermal ALTs for MCIC side interconnects
Comparing the typical (von Mises) stress contour plot at the critical corner of the joints and the cracks at the MCIC side interconnects, as shown in Figure 10 and dye penetration tests on failed reliability parts, we confirm the failure primarily initiates in the regions of high stress radiating from the intersection of the ceramic, side via, and solder.

Conclusions

Two board-level interconnect technologies have been reviewed for the MCIC applications within SSRC. Those include BGA and the MCIC side interconnects. Two groups of MCIC-BGA with different MCIC surface metallizations, Ag/Pd and Ag, were evaluated by thermal accelerated life tests. Coffin-Manson reliability curves were constructed. Combined with the bending test results, we conclude that the MCIC with silver surface metallization is more thermomechanically reliable than Ag/Pd. Micro-indentation developed in CTRL/SSRC can be used to determine the strength of MCIC solder interface with silver metallization. Three tests representing different sample processing were conducted for MCIC side interconnects. The reliability curves for two interconnect technologies are comparable. We found that, with reduced MCIC standoff height and larger MCIC size, the reliability of MCIC side interconnects can be maintained.
ACKNOWLEDGEMENTS

The authors would like to thank Robert Evans and Tim Murphy to provide MCIC backend process support. Claudia Jensen for the measurements of thermal cycling tests. Professor Jian Ku Shang for his micro-indentation technique developed in CTRL/SSRC. Rong-Fong Huang and Tom Wetteroth for the assistance of technology development in the early stage.

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INTERFACIAL REACTIONS IN LTCC MATERIALS

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ABSTRACT

State-of-the-art low temperature co-fired ceramic (LTCC) structures incorporate several types of embedded electronic components, including resistors, capacitors, filters, resonators, inductors, heat sinks, and sensors. Such complexity gives rise to intimate contact between diverse materials. When the laminated green LTCC structures are processed, typically at 800 °C – 900 °C, there are numerous opportunities for interfacial reaction. The resulting permutations and combinations form a large set of chemical systems which should be investigated, a task impractical for the short term; furthermore, new materials are continually being added to the list. To model LTCC interfacial reactions, with the aim of developing a method of treatment for general application, we have selected the system Ag-Bi2O3-Nb2O5-O. Certain aspects of interfacial reactions, as documented in the model system, may be extended to other systems in which dissimilar materials are in contact: 1. Interfacial reaction zones have fewer phases than would be predicted by the phase rule; 2. Although fewer phases are present, the sequence of reaction zones is consistent with the associated phase equilibrium diagram; 3. The chemical potential diagram, which can be derived from a thermodynamic model of the system, is useful in interpreting and predicting interfacial reaction zones.

BACKGROUND

Over the last two decades, LTCC technology has enabled major strides in cost reduction, miniaturization, performance enhancement, and reliability of electronic systems for communications, automotive and other applications. This trend is likely to continue as more electronic components are designed into LTCC packages. Typically, processing of LTCC materials occurs at 800 °C to 900 °C. The increased complexity of such systems means that the possibility of materials interactions during thermal processing at interfaces between dissimilar materials is also increased. The challenge for materials scientists is to devise a means for the treatment of chemical reactions occurring during thermal processing of LTCC. A method for interpreting or estimating interfacial reactions would be especially useful in the design of LTCC packages with new materials. It is our goal to explore the possibility of developing such a method [1].
APPROACH

A realistic treatment of interfacial reactions must include both equilibrium thermodynamics and reaction kinetics. The former defines the possibilities for phase formation at the interface, while the latter governs which of the alternative reactions actually occur, and the rates at which they occur. Equilibrium thermodynamic data are available for many relatively simple materials, such as pure metals and oxides [2], although there are comparatively few data for multicomponent materials. For some materials, reasonable estimates of thermodynamic parameters can be made based on simple mixing rules or other approaches [3]. By contrast, kinetic data are almost totally lacking for the majority of interfacial reactions which might occur in LTCC systems. The detailed kinetics of interfacial reaction processes are highly complex, and must include not only dissolution of unstable phases, but also nucleation and growth of new phases, as well as transport of reacting species by volume-, grain boundary- or surface diffusion. In some situations, gas-phase transport and transient liquids must also be considered. Possibly, in the absence of data, rough estimates of relevant kinetic parameters can be made on the basis of the very limited data available.

As a first step in the development of a comprehensive thermodynamic/kinetic, or “thermokinetic” approach, we have selected the system Ag-Bi₂O₃-Nb₂O₅-O for relatively detailed study. This system includes the Ag metallization typical of LTCC packages, as well as (Bi, Nb) oxide materials which form the basis for advanced dielectric materials currently under development. It has been observed that adverse reactions occur between metallic Ag and the oxides in the niobium-rich parts of the system [4], and so the model system provides an opportunity to investigate the relationship between equilibrium thermodynamics and reaction kinetics for a technologically important system.

THEORETICAL BASIS

The application of classical thermodynamic equilibrium theory [5] has benefited substantially from the development of modern computational approaches [6,7]. Rate theory has seen similar advances. Yet development of a combined thermokinetic approach has been limited to largely metallurgical situations [8]. It is therefore important to re-examine briefly the theoretical underpinnings necessary for a more general application.

It is a general observation that reaction sequences at interfaces contain fewer phases than the equilibrium phase diagram of the bulk system would predict [9]; it is essential to reconcile this apparent discrepancy. Korzhinsky [10] and Thompson [11] have given perhaps the most rigorous theoretical derivations of the relation between equilibrium thermodynamics and diffusion- or reaction-produced phase formation. The large chemical potential gradients at the interface between dissimilar materials provide the driving force for mass transport across the interface, and while this process is irreversible in an overall sense, Korzhinsky-Thompson theory allows application of equilibrium thermodynamics, provided certain assumptions are made. The first assumption is that within each small volume of the interfacial reaction zone, local equilibrium prevails. This requires that after the initial reaction, no phases in disequilibrium are in contact, and
that solid solutions show only continuous variations (in the absence of miscibility gaps). The second assumption is that relative to the other chemical components, the components which are diffusing across the interface may be regarded as thermodynamically mobile with respect to the local equilibrium volume. The chemical potentials of thermodynamically mobile components are defined by conditions external to the local equilibrium volume, i. e. they are externally controlled. Consequently, it can be shown that, at constant temperature and pressure,

$$\varphi = n - n_m$$  \hspace{1cm} (1)

where \( \varphi \) is the number of phases present in the general situation, \( n \) is the number of chemical components, and \( n_m \) is the number of mobile components \([11]\). Equation (1) reconciles the observation of fewer phases in reaction zones with the predictions of equilibrium bulk thermodynamics. Furthermore, the implication of equation (1) is that treatment of processes occurring in reaction zones is facilitated by consideration of the chemical potentials of the mobile components as intensive variables. Korzhinsky-Thompson theory fits well with reaction sequences observed in metallurgical and mineralogical systems. It has proved especially useful in interpreting reaction systems with more than four components \([12]\). For LTCC, it is important to determine the extent to which the theory can be applied at the relevant processing times and spatial dimensions.

**EXPERIMENTAL PROCEDURE**

Phase equilibrium studies were completed at 850 °C in air using powdered mixtures of Bi₂O₃, Nb₂O₅, and AgO as starting materials. Pellets were pressed, placed on MgO plates, and heated at 700-850 °C overnight with repeated grindings and homogenizations until no further changes in the x-ray patterns occurred. X-ray powder diffraction patterns were completed on a Philips 29 diffractometer using Cu Kα radiation and a graphite monochromator. Differential thermal analysis and thermogravimetric analysis experiments (DTA/TGA) were completed using a Mettler TA1 thermoanalyzer upgraded with Anatech digital control and data acquisition hardware and software.

Reaction couples were prepared by placing polished surfaces of Ag and BiNb₂O₁₄ together. The Ag was prepared from 99.99 % pure (metals basis), 2 mm thick sheet. The BiNb₂O₁₄ was prepared commercially by hot pressing to full density. Couples were held together during reaction at 850 °C in air by application of a uniaxial stress of approximately one MPa. Cross sections of reaction couples were prepared for characterization using scanning electron microscopy and energy dispersive x-ray analysis (SEM/EDS).

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1 Certain commercial equipment, instruments, or materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.
RESULTS and DISCUSSION

A provisional 850 °C isothermal phase diagram for the system Ag-Bi$_2$O$_3$-Nb$_2$O$_5$-O in air is shown in Fig. 1. Phases on the join Bi$_2$O$_3$-Nb$_2$O$_5$ have been characterized by Roth and Waring [13]. No phases were observed on the join Bi$_2$O$_3$-Ag. Three phases have been reported on the join Ag-Nb$_2$O$_5$ [14]. A ternary phase, Bi$_4$AgNb$_5$O$_{18}$, was suggested by [15]. We have confirmed the stability of this phase in the phase diagram by x-ray diffraction, and we have also determined its structure by neutron diffraction [16]. Liquid was observed only near the Bi$_2$O$_3$ corner of the diagram. The system is especially complicated in the Nb$_2$O$_5$-rich part; investigation of this part is not yet complete, as indicated by the dashed lines. If the general distribution of tie lines (and in particular, the AgNbO$_3$ – BiNbO$_4$ tie line) is assumed to be correct, then an Ag/BiNb$_3$O$_{14}$ interface (indicated by the dotted line in Fig. 1) should be unstable and yield evidence of reaction.

Micrographs of an Ag/BiNb$_3$O$_{14}$ interface heated at 850 °C in air for 20 h are shown in Fig. 2. A well-defined reaction zone at the interface is indicated by the Ag L$_\alpha$ x-ray map of Fig. 2b. This reaction zone extends ~ 80 μm from the edge of the Ag. In order to apply Korzhinsky-Thompson theory, we have prepared a qualitative chemical potential diagram based on Fig. 1, as shown in Fig. 3, by assuming thermodynamic mobility of both Ag and Bi$_2$O$_3$ relative to Nb$_2$O$_5$. The diagram in Fig. 3 predicts that, in general, reaction zones between unstable pairs in the Ag-Bi$_2$O$_3$-Nb$_2$O$_5$ system should be monophasic in situations where both Ag and Bi$_2$O$_3$ are mobile. However microstructural observations (to be described in more detail in a subsequent publication) indicate that the reaction zone in Fig. 2 is biphasic. Based on the geometry of the reaction zone relative to the unreacted Ag, it is clear that Ag has been transported across the interface and into the

![Figure 1. Provisional isothermal phase diagram of the system Ag-Bi$_2$O$_3$-Nb$_2$O$_5$-O in air at 850 °C. Dotted line indicates Ag/BiNb$_3$O$_{14}$ reaction couple.](image-url)
Figure 2. SEM image (a) and Ag L_{\alpha} x-ray map (b) of Ag/BiNb_5O_{14} reaction couple heated at 850 °C, 20 h in air, with an applied uniaxial compression of ~ 1 MPa.
Figure 3. Chemical potential diagram based on Fig. 1, with the assumption of thermodynamically mobile Ag and Bi$_2$O$_3$.

BiNbsOu, and as Ag was transported, the edge of the Ag receded. EDS measurements indicated no measurable Bi or Nb in the Ag. These observations suggest that the only mobile component was Ag. A chemical potential diagram based on Fig. 1, which assumes mobility of only Ag, is shown in Fig. 4. As can be seen in Fig. 4, under conditions of Ag mobility, biphasic reaction zones are the general feature expected at interfaces between unstable pairs in the Ag-Bi$_2$O$_3$-Nb$_2$O$_5$ system, in agreement with observations noted above in the reaction zone of Fig. 1.

Kinetic data on interfacial reactions in the model system Ag-Bi$_2$O$_3$-Nb$_2$O$_5$ can be obtained thermogravimetrically. Fig. 5 shows reactions occurring in a powdered AgO/Bi$_2$O$_3$/Nb$_2$O$_5$ starting material during the initial heat treatment. As the sample was heated, a weight loss occurred over the range 160 °C to 200 °C, which corresponds to the reaction,

$$2 \text{AgO} \rightarrow \text{Ag}_2\text{O} + \frac{1}{2} \text{O}_2 \quad (2).$$

Next a weight loss occurred over the range 400 °C to 430 °C, according to the reaction,

$$\text{Ag}_2\text{O} \rightarrow 2 \text{Ag} + \frac{1}{2} \text{O}_2 \quad (3).$$

As the temperature increased further, the sample began to gain weight beginning at about 500 °C as the silver reacted with Bi$_2$O$_3$ and Nb$_2$O$_5$:
Figure 4. Chemical potential diagram based on Fig. 1, with the assumption of thermodynamically mobile Ag.

Figure 5. Thermogravimetric analysis of reactions in a powdered mixture of AgO, Bi₂O₃, and Nb₂O₅ with progressive heating in 100% O₂.
\[ 2 \text{Ag} + 5 \text{Bi}_2\text{O}_3 + 4 \text{Nb}_2\text{O}_5 + \frac{1}{2} \text{O}_2 \rightarrow 2 \text{Bi}_5\text{AgNb}_4\text{O}_{18} \] (4).

Interfacial reactions involving Ag with oxide LTCC materials are all similar to (4) in that oxygen is taken up as the metallic Ag reacts to form Ag$_2$O-containing product phases. By monitoring the weight gain as a function of time, an indication of the interfacial reaction kinetics can be obtained, as in Fig. 6. The weight gain curve in Fig. 6 is related to the rate of reaction of Ag with a pellet of sintered BiNb$_2$O$_{14}$ having open porosity [1]. This experiment was completed at 850 °C in 100% O$_2$. A reaction zone with many times the width of that in Fig. 1 was produced, presumably due to a combination of the higher P$_{O_2}$ with the opportunity for surface diffusion presented by the open porosity. By contrast, only the relatively slower processes of grain boundary and volume diffusion were allowed by the relatively dense BiNb$_2$O$_{14}$ of the experiment in Fig. 1. All thermogravimetric curves observed to date for reaction of Ag with (Bi,Nb)-oxide materials are similar in form; however as the curve in Fig. 6 shows the largest observed weight gain, it provides the most useful example for purposes of illustration. The data in Fig. 6 can be approximately fitted by a parabolic curve of the form

\[ x^2 = K't \] (5),

where \( x \) is the thickness of the reaction product layer (assumed proportional to the mass of O$_2$ gained), \( K' \) is an apparent diffusion coefficient which represents the sum of the mass transport processes taking place, and \( t \) is time [1]. A parabolic fit of this type is consistent with a reaction rate being limited by transport (of Ag) through a planar product.

![Figure 6. Thermogravimetric analysis of reaction at an Ag/porous BiNb$_2$O$_{14}$ interface at 850 °C, in 100% O$_2$ [1].](image-url)
layer [17]. In detail, however, it has been observed that use of higher order terms significantly improves the fit. Research is being directed at the extraction of relevant diffusion and reaction parameters from data of the type in Fig. 6. This will form the initial kinetic database to be combined with the thermodynamic database for a comprehensive thermokinetic model of the system Ag-Bi$_2$O$_3$-Nb$_2$O$_5$-O.

**CONCLUSIONS**

Experiments in the model system Ag-Bi$_2$O$_3$-Nb$_2$O$_5$-O have shown the applicability of Korzhinsky-Thompson theory to the development of reaction zones at Ag/BiNb$_2$O$_4$ interfaces. It is likely that this approach, in which equilibrium thermodynamic data are applied to reaction interfaces via the concepts of local equilibrium and thermodynamic mobility, can be applied to other LTCC systems, as well. Through the use of chemical potential diagrams it is possible to predict the topology of interfacial reaction zones, and to interpret data on the extent and identity of phases forming at the interface in terms of the kinetics of diffusion, nucleation, growth and dissolution. Data on the model system Ag-Bi$_2$O$_3$-Nb$_2$O$_5$-O will offer an opportunity to develop a detailed thermokinetic model of interfacial evolution, which ideally will serve as a template for more general application.

**ACKNOWLEDGEMENTS**

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Thermoelectric Materials
THERMOELECTRIC MEASUREMENTS

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ABSTRACT

This paper describes thermoelectric devices and measurements of thermoelectric materials. The governing equations describing the efficiency of generators based on these materials are reviewed utilizing the Onsager relations as a starting point. The identification of important material properties is extracted from these equations, and a description of some of the measurement issues are discussed. Additional analysis of the data is described in light of the governing equations.

INTRODUCTION

The study of thermoelectrics is multidisciplinary in nature including studies of chemistry, condensed matter physics, and engineering. Through macroscopic transport measurements, the figure of merit can be assessed for materials of interest, and further insight can be obtained into the microscopic properties of the samples. Our approach to studying new materials for thermoelectric applications has largely been exploratory in nature, however, with an increased understanding of the microscopic properties several key avenues are being sought toward the development of highly efficient materials. For such insight, measurements of thermoelectric power, electrical conductivity, and thermal conductivity should be made, all on the same sample. This is necessary to obtain accurate determination of the unitless figure of merit, $ZT = S^2 \sigma / \kappa T$, where $S$ is the thermoelectric power, $\sigma$ is the electrical conductivity, $\kappa$ is the thermal conductivity, and $T$ is temperature. Each of these material parameters can be obtained through a variety of measurement techniques including methods for obtaining $ZT$ directly. Additional insight can be obtained through Hall Effect and scanning probe measurements which are also useful in determining carrier concentrations, carrier mobilities, and sample uniformities. Toward the engineered development of these materials into applications, more measurements are needed at the device level, which includes contributions from contact resistances (both thermal and electrical), and additional thermal losses when large temperature gradients are involved. The steady state and non-steady state models of these devices can be utilized both in device design, and in the analysis of measured results. We have developed several measurement techniques for characterizing new thermoelectric materials and devices, including temperature dependent electrical conductivity, thermoelectric power, thermal conductivity, and Hall Effect measurements. In addition, the results from room temperature scanning probe measurements have given further insight into accurate geometry measurements on the samples, sample uniformities, and contact resistances. By starting with the Onsager relations, it is possible to formulate the fundamental flow equations connecting the measurable fluxes and forces in terms of material properties. The governing of experimental investigations into new thermoelectric materials will be extracted from the flow equations, and followed by descriptions of the measurement systems used in characterizing the samples and thermoelectric devices.
Thermoelectric devices are heat pumps that can be used for creating a temperature gradient across the device, when electrical power is supplied to its terminals. Conversely, when supplying a temperature gradient across the device, a voltage difference will be generated across its terminals. These devices can thus be utilized either as a cooling device, by supplying electrical power, or as a power generation device, by supplying thermal power. In the fabrication of thermoelectric generators (coolers), a common goal has been the design of a device that yields the highest efficiency (coefficient of performance) possible.

The heat flow and electrical charge flow through the device are macroscopically measured flows of energy or particles through the materials. In 1931, Onsager developed a method to relate the flows of matter or energy within a system to the forces present. In this method the forces are assumed to be small such that a linear relationship between the forces, \( X_i \), and corresponding flows, \( J_i \), can be written as

\[
J_1 = L_{11}X_1 + L_{12}X_2 + \ldots + L_{1n}X_n \\
J_2 = L_{21}X_1 + L_{22}X_2 + \ldots + L_{2n}X_n \\
J_3 = L_{31}X_1 + L_{32}X_2 + \ldots + L_{3n}X_n
\]

or

\[
J_i = \sum_{m=1}^{n} L_{im}X_m \quad (i = 1, 2, 3, \ldots n)
\]

The coefficients \( L_{im} \) are most easily determined by considering the rate of entropy, \( S \), produced per unit time, during an irreversible process which is equal to the summation of the products of flows and forces or

\[
\frac{dS}{dt} = \sum_i J_i X_i
\]

Utilizing Gibbs equation, it is then possible to write the electrical current, \( J \), and the heat current \( J_Q \) as

\[
J = -\frac{L_{11}}{T} \nabla \mu + L_{12} \nabla \left( \frac{1}{T} \right) \\
J_Q = -\frac{L_{21}}{qT} \nabla \mu + \frac{L_{22}}{T^2} \nabla V
\]

where the electrochemical potential, \( \mu \), is \( \mu = \mu + qV \) with \( \mu \) as the chemical potential, and \( V \) is the electrostatic potential, and \( q \) is the charge of the particle (\( 1.602 \times 10^{-19} \) C for electrons). The \( L_{ij} \) coefficients follow the Onsager relationship of \( L_{ij} = L_{ji} \).
\( L_{11} = \frac{T_0\sigma}{q^2} \)

\( L_{12} = L_{21} = \frac{\sigma T^2 S}{q} \)

\( L_{22} = T^2 (\kappa + T_0\alpha S^2) \)

where \( \kappa \) is the thermal conductivity at zero current. Combining these gives

\( J = -q \left[ \nabla \left( \frac{\Pi}{e} \right) + SVT \right] \), and \( J_Q = STJ - \kappa VT \) \hspace{1cm} (6)

In the condition of zero temperature gradient (\( \nabla T = 0 \)), equation (6) gives

\( J_Q = STJ \) or \( \frac{J_Q}{J} = ST = \Pi \) \hspace{1cm} (7)

which defines the Peltier coefficient, \( \Pi \). A simplified view of the heat absorption or emission at a junction between two materials having different thermopowers with current flowing through the junction is viewed on an energy band diagram that includes the metal to semiconductor junctions of a typical thermoelectric device configuration.

Figure 1. Peltier heat absorption and emission at metal semiconductor junctions in a thermoelectric device used as a cooler.
These junctions are shown in Figure 1 where it is shown that electrical current is forced to flow through the device by applying an external voltage. This causes charge carriers to flow from the top of the device to the bottom of the device in each of the legs (p-type and n-type). As an electron passes from the metal into the n-type semiconductor as shown in the upper right of the figure, it must absorb the energy difference between the average energy in the metal, $\Delta E_m$, and the average energy in the semiconductor $\Delta E_{n}$ above the Fermi level, or:

$$\Pi_{m_n} = \frac{1}{|q|} \left[ \Delta E_n + (E_c - E_F) - \Delta E_m \right]$$

(8)

Similarly, when an electron hole pair is generated at the metal to p-type semiconductor junction in the upper right of Figure 1, the energy absorbed is:

$$\Pi_{m_p} = \frac{1}{|q|} \left[ \Delta E_p + (E_F - E_c) + \Delta E_m \right]$$

(9)

With correspondingly formulated quantities for the heat emission at the two lower contacts shown in Figure 1. The average energy of the carriers in the semiconductors and metals will depend on the local temperature.

**THERMEOELECTRIC GENERATOR**

The standard configuration of a thermoelectric generator is shown in Figure 2, which shows electrical current being supplied to a load resistance, $R_L$ when a temperature gradient ($T_h - T_c$) is supplied across the generator. In this case, heat is forced to flow from the top to the bottom of the device by applying a temperature gradient across the device with the hot side on top as shown in Figure 2. Again, in this case, all charge carriers flow from the top to the bottom of the device, thus there is a buildup of positive charge at the bottom of the p-type leg, and a buildup of negative charge at the bottom of the n-type leg. This yields a voltage across the terminals of the device which can be used to supply power to a load resistance, $R_L$.

![Figure 2. Common design of a single junction thermoelectric generator [2].](image)
The thermoelectric efficiency of this generator is defined as the ratio of the power, $P_o$, delivered to the load resistance, $R_o$, over the power delivered to the generator in the form of the rate of heat flow through the generator, $Q_h$, or:

$$\eta = \frac{P_o}{Q_h} \quad (10)$$

The power delivered, $P_o$, is simply $P_o = I^2R_o$, and the heat flow through the device, $Q_h$ is found by using the thermal conductance, $K = (K_\sigma + K_p)$, the Seebeck coefficient, $S_{pm} = (S_p - S_n)$, the resistance of the legs, $R = R_a + R_p$, and the contact resistance, $R_c = R_{ch1} + R_{ch2} + R_{cc1} + R_{cc2}$ as shown in Figure 2.

$$Q_h = K\Delta T + ST_Hl - \frac{1}{2}I^2(R + R_c) \quad (11)$$

Defining the ratio of contact resistance to thermoelectric material resistance as $\delta$, and the Carnot efficiency, $\eta_c$ as

$$\delta = \frac{R_c}{R} \quad \text{and} \quad \eta_c = \frac{\Delta T}{T_H} \quad (12)$$

defining

$$\mu = \sqrt{(1 + \delta)^2 + (1 + \delta)ZT_{av}} \quad (13)$$

then the efficiency, $\eta$, can be found as

$$\eta = \frac{\mu\eta_c}{ZT_h + (\mu + 1 + \delta)\frac{(1 + \delta)\eta_c}{2}} \quad (14)$$

where $ZT_{av}$ in (13) is the figure of merit for the generator and is equal to:

$$ZT_{av} = \frac{S^2\sigma}{\kappa} \quad (15)$$
This shows that the efficiency of the generator is dependent on the figure of merit and the material properties of electrical conductivity, $\sigma$, thermoelectric power, $S$, and thermal conductivity, $\kappa$. Equation (14) further shows that the efficiency is also dependent on the temperature gradient, through $\eta_\iota$, and on the contact resistance through $\delta$. A plot showing the dependence of $\eta$ on $ZT_{av}$ for various values of $\delta$ is shown in Figure 3.

![Figure 3](image)

**Figure 3.** Thermoelectric generator efficiency versus $ZT_{av}$, for various contact resistances ($\delta = R_C/R$).

It is possible to further develop this equation through an analysis of Fermi-Dirac statistics on each of the three parameters. Using a one band model, for a heavily doped $n$-type sample measured in the $x$ direction yields:

$$\sigma = q\mu_x n = \frac{q\mu_x}{2\pi^2} \left( \frac{2k_BT}{h^2} \right)^{3/2} \sqrt{m_xm_ym_z} \int F_{1/2}$$

where $m_x$ is the mobility in the $x$ direction, $m_x$, $m_y$, and $m_z$ are the effective mass components, and $F_{1/2}$ is the Fermi-Dirac function of order $1/2$. The Fermi-Dirac function is defined as:

$$F_i = F_i\left(\xi^*\right) = \int_0^\infty \frac{x^i}{e^{x-\xi^*}+1} \, dx$$

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and $\zeta^* = \frac{\zeta}{k_B T}$ is the reduced chemical potential relative to the conduction band edge.

$$S = -\frac{k_B}{q} \left( \frac{s + 2}{s + 1} \frac{F_{s+1}}{F_s} - \zeta^* \right)$$  \hspace{1cm} (18)$$

$$\kappa = \kappa_e + \kappa_L$$
$$\kappa = \frac{k_B \mu_x \hbar^2}{q 4 \pi^2} \left( \frac{2k_B T}{\hbar^2} \right)^{3/2} \left( \sqrt{m_x m_y m_z} \right) F_{3/2} \left[ \frac{(s + 3) F_{s+2}}{(s + 1) F_s} - \frac{(s + 2)^2 F_{s+1}^2}{(s + 1)^2 F_s^2} \right] + \kappa_L$$ \hspace{1cm} (19)$$

where $s$ is the scattering parameter. For lattice scattering in a non-polar material $s = 0$, in a polar material $s = \frac{1}{2}$, and for ionized impurity scattering $s = 2$.

**MEASUREMENTS**

Measurement of these three parameters: $S$, $\sigma$, and $\kappa$ pose a number of challenges. In the case of electrical conductivity, two configurations that are commonly used for bulk materials is the two probe and four probe technique shown in Figure 4.

![Two probe configuration](image1)

![Four probe configuration](image2)

**Figure 4.** Two measurement configurations for electrical conductivity on bulk samples.

The two probe configuration the voltage meter measures the voltage drop across the sample plus the voltage drop across the contact resistances, and the drop across the length of wire between the voltage meter and the sample. Since the total current being supplied to the sample also passes through these wires, and the contacts, the voltages across these resistances can be appreciable, particularly for low resistance samples. In the four probe configuration, however, the voltage meter is connected to the sample by two additional wires. Since the input resistance to the voltage meter is large (typically $> 10 G\Omega$), the
current through these wires will be negligible, thus the voltage measured will simply be the voltage drop along the length of the sample between the voltage probes. For this reason the four probe configuration is most often utilized. When taking this measurement the voltage contacts should be small to minimize perturbation of the electric field in the sample. If the voltage lead contact resistance is very large, however, then the amount of noise in the voltage measurement can become appreciable. These contacts are often placed on the sample by hand using a conductive paste. With careful mounting, these contacts might be made at the 0.4mm diameter geometry as shown in Figure 5 for a sample with a 2mm width and 6mm length. If the conductive paste used for making these contacts is of high electrical conductivity, such that it can be assumed infinite compared to the sample, then no voltage drop across the 0.4mm diameter of the contact should exist. The questions was thus raised as to whether the voltage being measured is the voltage drop across the 1.6mm of the sample length between the voltage probes, or the midpoint to midpoint distance of 2mm between the voltage probes shown in Figure 5. Since this would correspond to a 20% difference in the measured electrical conductivity of the sample, it can be a significant source of error.

![Image](image_url)

Figure 5. Four probe electrical conductivity configuration with voltage lead contacts of 400μm diameter on a 2mm wide by 6mm long bulk sample.

To investigate the proper probes spacing to use, we measured the voltage profile along the length of the sample and compared the measurements to those obtained with the four probe configuration using both the inside edge to inside edge, and midpoint to midpoint probe spacing. This was investigated on a sample of bismuth telluride mounted with voltage contacts of approximately 350μm diameter as shown in Figure 6. At a current of 10mA, the four probe configuration gave electrical conductivities for the probe spacing of inside-edge to inside-edge, midpoint to midpoint, and outside-edge to outside-edge as shown in Table 1.
Figure 6. Sample used for measuring the electrical conductivity by scanning probe and fixed four probe techniques.

The voltage was then measured between the grounded end of the sample, and a traveling probe that was scanned along the length of the sample as shown in Figure 6. The slope, $dV/dx$, of the voltage versus traveling probe position can then be used to calculate the electrical conductivity as:

$$
\sigma = \frac{I}{V} \left( \frac{ps}{A} \right) = \frac{1}{A} \left( \frac{1}{dV/dx} \right)
$$

(20)

where $I$ is the electrical current (10mA), and $A$ is the cross-sectional area of the sample (5.04mm²). The sample was then measured at four different current levels using the scanning probe technique. Plots of the measured data are shown in Figures. The data were fit to a straight line for the data over the full length of the sample (~8.5mm), and a second fit for just the middle 2.5mm of the sample. The second fit was used to avoid thermal influences on the data caused by Peltier heating and cooling at the current contacts at the ends of the sample.

Table 1. Four probe measurements of electrical conductivity on the sample shown in Figure 6, with a current of $I = 10$mA.

<table>
<thead>
<tr>
<th>Probe Spacing</th>
<th>Probe Spacing (mm)</th>
<th>Electrical Conductivity (S/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outside-edge to outside-edge</td>
<td>4.9</td>
<td>1114</td>
</tr>
<tr>
<td>Midpoint to midpoint</td>
<td>4.55</td>
<td>1029</td>
</tr>
<tr>
<td>Inside-edge to inside-edge</td>
<td>4.2</td>
<td>955</td>
</tr>
</tbody>
</table>
The voltage drops at the ends of the sample are due to the contact resistance at the current electrodes.

Figure 7. Measured data on the sample shown in Figure 6 from the scanning voltage probe technique at a current of 1 mA.

Figure 8. Measured data on the sample shown in Figure 6 from the scanning voltage probe technique at a current of 5 mA.
Figure 9. Measured data on the sample shown in Figure 6 from the scanning voltage probe technique at a current of 10mA.

Figure 10. Measured data on the sample shown in Figure 6 from the scanning voltage probe technique at a current of 20mA.
Comparing these results to those obtained in Table 1, the best agreement between the measurement techniques occurs for calculations based on the midpoint to midpoint voltage probe spacing.

Variations can exist among samples even if they are cut from the same ingot. It is, therefore, important to measure all of the parameters (S, \( \sigma \), and \( \kappa \)) on the same sample. To accomplish this, we have adopted a pulsed technique first described by Maldonado [3] and later modified to include a four probe configuration, electrical conductivity measurements, and computer control of the system [4], and most recently designed for four samples to be measured simultaneously [5, 6]. The samples are mounted so that S, \( \sigma \), and \( \kappa \) can be measured concurrently on the sample. A challenge associated with these measurements is the thermal losses that exist as described in Figure 11.

![Diagram of thermal losses](image)

**Figure 11.** Thermal losses caused by conduction through the wires, convection through the surrounding air, and radiation.

These losses can be quantified in the following equations for conduction, convection, and radiation losses respectively.

\[
\dot{Q}_{\text{cond}} = \kappa (T_1 - T_0) \frac{A}{L}
\]

(21)

\[
\dot{Q}_{\text{gas}} = a \frac{\gamma + 1}{\gamma - 1} \sqrt{\frac{R}{8\pi}} \frac{P}{\sqrt{MT}} (T_1 - T_0) = 0.03 P_{\text{max}} (T_1 - T_0) \quad \text{\text{\(\text{W/cm}^2\)}}
\]

(22)

\[
\dot{Q}_{\text{rad}} = \frac{\xi e}{2 - e} \left( T_1^4 - T_0^4 \right)
\]

(23)

where \( \xi = 5.67 \times 10^{-8} \frac{\text{W}}{\text{m}^2 \cdot \text{K}^4} \) is the Stephan-Boltzmann constant. In the case of a 1 cm long cylindrical sample with a diameter of 4 mm and having a thermal conductivity of
1 W/m-K, the thermal conductance through the sample is 1.26 mW/K. For a 25 μm diameter copper wire that is 10 cm long connected to the sample, the thermal conduction through the wire is approximately 2 μW/K. Losses caused by convection at a pressure of 10^4 Torr are approximately 3 μW/K for a 1 cm² heat source. The radiation losses for a 1 K temperature difference between the hot side temperature, and the sample's surroundings are shown as a function of sample stage temperature in Figure 12.

![Graph showing radiation losses per square centimeter of surface area](image)

Figure 12. Radiation losses per square centimeter of surface area, for a sample with an emissivity of 1.0 and a temperature of T_i = T_0 + 1.

This exercise shows that thermal losses are dominated by the radiation losses at the higher temperatures and can become significant relative the thermal conductance through the sample. This most significantly effects the thermal conductivity measurement since it is measured as the power supplied to a small heater on one end of the sample over the resulting temperature gradient across the sample. With these additional thermal losses, more power must be supplied to the small heater, resulting in a measured thermal conductivity that is higher than the actual thermal conductivity of the sample. Measured thermal conductivity that exhibits a ~T^3 increase in thermal conductivity at the higher temperatures is often associated with the radiation losses as shown in Figure 12.

Additional information about the samples can be extracted from the data as shown in equation (18), where the thermopower of the sample is shown to depend only on the reduced chemical potential ξ*. We have thus, developed a program for iteratively solving (18) for different values of ξ* with the results shown in Figure 13 for a scattering parameter of s = 1/2.
This allows one to determine the position of the chemical potential (or Fermi level) relative to the conduction band edge (negative values correspond to the Fermi level being located inside the bandgap). As an example, the above described measurement system was utilized to collect the thermoelectric power on bismuth telluride samples, and some new materials consisting of lead-antimony-silver-tellurium (L-A-S-T) as shown in Figure 14. Utilizing this method with the temperature dependent data, a plot of the reduced Fermi level position is shown in Figure 15 where it is seen that the chemical potential begins at a location of several $k_B T$ inside the conduction band at lower temperatures, and gradually moves toward the conduction band edge. As the Fermi level enters the bandgap, a two band model should be used to account for contributions from holes in the valence band from electron-hole generation.

Through Hall effect measurements, the carrier concentration can be measured, which can then be used to determine the effective mass of the carriers through

$$n = \frac{1}{2\pi^2} \left( \frac{2k_B T}{\hbar^2} \right)^{3/2} \sqrt{m_x m_y m_z} F \gamma_2$$

(24)
Figure 14. Thermoelectric power on Bi$_2$Te$_3$ and L-A-S-T samples.

Figure 15. A plot of the reduced Fermi energy level as a function of temperature as determined from measured data and equation (18).
ACKNOWLEDGEMENTS

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HIGH TEMPERATURE POWER FACTOR MEASUREMENT SYSTEM FOR THERMOELECTRIC MATERIALS

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ABSTRACT

A new computer-controlled thermoelectric measurement system is presented to characterize the thermoelectric properties of new materials, primarily at high temperature (up to 800K). Thermoelectric research at high temperature is of interest since materials with high thermoelectric efficiency at high temperatures have potential applications in power generation. Using this system, we can study the new materials properties over a very broad temperature range. This system was designed to measure the thermoelectric power through a slope measurement technique, and electrical conductivity in the standard four-probe configuration. Various ways of measuring the electrical conductivity are investigated, for instance through I-V sweeping, flipping the source current directions, and ac techniques. Here we present the use of this high temperature system in studying the properties of new materials over a very broad temperature range (80-800K). Various reference materials for thermoelectric power and electrical conductivity are characterized in this system and show good agreement with the reference data.

Renewed interest in the field of thermoelectricity (TE) has stimulated scientists in the TE community to investigate new aspects of this research, for instance, new materials synthesis techniques, new material characterization systems, and new ways of designing thermoelectric materials. Recently, many studies have concentrated on thermoelectric power generation applications. This is due to the increasingly important issue of recovery waste heat, e.g. in automobiles and systems that output large amounts of waste heat.

INTRODUCTION

A new computer-controlled thermoelectric measurement system is built to measure the power factor ($S^2\sigma$, $S$ is thermoelectric power and $\sigma$ is electrical conductivity) of materials as a function of temperature (up to 800K). The setup of this high temperature measurement system will be described in another paper (1). This paper will explore the investigation of new quaternary thermoelectric materials using this high temperature (HT) measurement system. Figure 1 and 2 show the comparison of the measured and reference data for a molybdenum sample. The measurements show very good agreement to the reference with less than 3% of error percentage.
Figure 1 The comparison of the thermopower of molybdenum between the reference (2) and high-temperature system.

Figure 2 The comparison between the reference (3) and measured electrical resistivity of molybdenum.
RESULTS AND DISCUSSIONS

A sample from the new LAST series of quaternary materials is measured. The LAST series samples consist of lead, antimony, silver and tellurium composition. These materials are cubic structure with distortion. The thermopower increases linearly with temperature while the electrical conductivity decreases dramatically with temperature as shown in Figure 3. The HT data is overlapped with the data obtained from the 4-sample measurement system. The 4-sample measurement system is a well-established low temperature (80-400K) ZT measurement system (4), also developed in the lab. At room temperature, the electrical conductivity is about 1000 S/cm and the thermopower is about -150 μV/K. This gives a power factor of 22.5 μW/K²·cm. At 700K, the electrical conductivity reduces to 200 S/cm and the thermopower reaches -300 μV/K. This gives a power factor of 18 μW/K²·cm. Another sample from the same series, with slightly higher silver composition, was measured and the result is shown in Figure 4. With the addition of silver, the electrical conductivity at room temperature is doubled as compared to the previous sample, while yielding almost the same thermopower. The power factor is 28.8 μW/K²·cm at room temperature and 23.5 μW/K²·cm at 700K.

![Figure 3 LAST series data obtained from the HT and 4-sample system.](image)
Figure 4 LAST series (with slightly higher silver composition) data obtained from the HT and 4-sample system.

Figures 5, 6 and 7 show the measurement results of different sections in a LAST series. The sample was grown in ingot and was cut to three different sections (See Figure 8). Figure 5 shows the electrical conductivity of the three sections. The samples have metallic behavior since the conductivities reduce as the temperature increases. Figure 6 shows the thermopower of the three samples. The thermopower values increase linearly with temperature until around 600-700K. The power factors of the three samples are shown in Figure 7.

Figure 5 Electrical conductivity of LAST samples and the sample ID is KF2242R2 with A, B and C sections.
Figure 6 Thermopower of LAST samples and the sample ID is KF2242R2 with A, B and C sections.

Figure 7 Power factor of LAST samples and the sample ID is KF2242R2 with A, B and C sections.
The high temperature system does not include the thermal conductivity measurement due to large radiation loss at high temperatures. In order to estimate the figure of merit, $Z_T$, of the material, a theoretical calculation is included here to roughly derive the thermal conductivity of the materials based on the existing power factor data and thermal conductivity data measured with the 4-sample (low-temperature) system.

The electrical conductivity can be expressed as $\sigma = n e^2 \langle \tau \rangle / m_e$, and the electronic thermal conductivity is $\kappa_e = L_0 T = \lambda (k^2 / e^2) \sigma T$ where

$$\lambda = \frac{\langle \tau \rangle (E^2 \tau) - \langle E \tau \rangle^2}{k^2 T^3 \langle \tau \rangle^2}$$

and $L$ is a pure number and $L = L(k^2/e^2)$ is the Lorentz number.

For a non-degenerate semiconductor, the relaxation time is $\tau = a E^2$ so

$$\langle \tau \rangle = a \Gamma(\frac{3}{2} - s) / \Gamma(\frac{3}{2})$$
$$\langle E \tau \rangle = a k T \Gamma(\frac{3}{2} - s) / \Gamma(\frac{3}{2})$$
$$\langle E^2 \rangle = a k^2 T^2 \Gamma(\frac{3}{2} - s) / \Gamma(\frac{3}{2})$$

Since $I(1+x) = x I(x)$, so $L = \frac{3}{2} - s$. $s$ is the scattering parameter and for various scattering mechanisms, the $s$ value is different. For scattering by the acoustical modes, $s = \frac{1}{2} (L = 2)$, and for ionized impurities scattering $s = -3/2 (L = 4)$.

For a fully degenerate semiconductor, a better approximation is needed to obtain the Lorentz number $L$. We have $\langle \tau \rangle (E^2 \tau) - \langle E \tau \rangle^2 = \frac{1}{4} \pi^2 k^2 T^4 \langle \tau \rangle^2$ so $L = 1/3 \pi^2 = 3.289$ and $L = 2.44x10^8 V^2/K^2$. If a semiconductor which is degenerately doped but not fully degenerate, we can assume $L = 2.15$ and thus $L = 1.596x10^8 V^2/K^2$.

For the cubic materials, the latter Lorentz number is more suitable for calculating the electronic contribution of the thermal conductivity. However, since the materials are very highly doped, both Lorentz numbers are used for calculation comparisons.

Figure 9 shows the total thermal conductivity of sample KF2242R2A as measured in the 4-sample system from 80-400K. Figure 10 shows the calculated electronic thermal conductivity based on the measured electrical conductivity values measured from the 4-sample and HT systems. Since the total thermal conductivity is known from 80-400K. We can approximate the lattice term for both L values and it is shown in Figure 11.
Figure 9 The total thermal conductivity of KF2242R2A from the 4-sample system in Hogan's lab.

Figure 10 The electronic thermal conductivity of KF2242R2A calculated from the electrical conductivity and with two different Lorentz numbers.
Figure 11 The lattice thermal conductivity of KF2242R2A is calculated from subtractions of electronic thermal conductivity from the total thermal conductivity. These data are calculated through the equations of the sixth polynomial fit of the electronic thermal conductivity and the fourth polynomial fit of the total thermal conductivity.

The two basic scattering mechanisms in conduction are the lattice scattering and impurity scattering. Lattice scattering is when the carriers are scattered by vibration of the lattice. This vibration results from the temperature of the material. Thus, as the temperature increases, lattice scattering is dominant and causes the carriers’ mobility to decrease. Impurity scattering, on the other hand, is dominant at low temperature. At low temperature, the thermal lattice vibration is low and the carriers are more likely to be scattered by charged ions (impurities) than by lattice vibrations.

In Figure 12, the lattice thermal conductivities are assumed to be constant at high temperatures because lattice scattering is dominant. Once the lattice thermal conductivities are estimated, the electronic thermal conductivities can be added to obtain the total thermal conductivities as shown in Figure 13. Finally, the $ZT$ of the material can be estimated as shown in Figure 14.
Figure 12 The lattice thermal conductivity of KF2242R2A with curve fit till 700K.

Figure 13 The total thermal conductivity of KF2242R2A with two different Lorentz number.
CONCLUSION

A high temperature thermoelectric transport measurement system has been successfully employed to investigate new quaternary thermoelectric materials. The measurements reveal that these materials are n-type semiconductors with metallic behavior. A power factor of more than 20\(\mu W/K^2\cdot cm\) is measured at high temperature. Since the thermal conductivity of these materials decreases with increasing temperatures, a ZT of approaching or larger than unity is possible. This system is used to study the various alloying trends and the variation within an ingot of new materials.

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Overview of properties of "metallic" Na$_x$Co$_2$O$_4$ thermoelectric materials

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Abstract:
Since the thermoelectric properties of transition-metal oxide NaCo$_2$O$_4$ were first reported by Terasaki in 1997, extensive research work has been conducted on this system of ceramic oxide thermoelectric materials. Efforts to improve the thermoelectric properties through doping or new synthesis approaches have been investigated. More recently, efforts have been expended in theoretical investigations in order to explain the coexistence of small resistivity values and relatively large thermopower values simultaneously in these materials, which is not apparent from conventional free-electron theory. Current studies indicate the strong electron correlation and spin entropy may be the main reasons behind the enhanced thermopower of this "metallic-like" ceramic oxide, Na$_x$Co$_2$O$_4$. Recently, superconducting behavior under 5K was reported in the hydrated form of this oxide Na$_x$Co$_2$O$_4$·yH$_2$O. In this paper a review of the newest research developments are presented, and as well our own results and future research directions are also discussed.

1. Introduction
Thermoelectric (TE) materials can convert heat into electrical energy through Seebeck effect; and conversely electricity energy can be converted into thermal energy via Peltier effect. TE devices exhibit high stability, quiet operation (without moving parts) and the ability to exhibit small-scale localized cooling/heating. However, the low efficiency of current TE devices make the applicable somewhat "niche" applications where the high reliability or specific application makes the selection of these devices favorable, even though they may exhibit low conversion efficiencies (≈ 6-7%). Present applications of TE materials and devices are based on two aspects, one for power generation, such as NASA's deep space probes (Voyager and Cassini), and the other one for solid state cooling, such as computer chips, optoelectronic devices (IR detectors) or the more readily available TE picnic coolers.

The performance of the thermoelectric materials, which is proportional to the device efficiency, is related to the dimensionless figure-of-merit (FOM) which is defined as $ZT = \alpha^2 T / \rho (\kappa_L + \kappa_e)$, where $\alpha$ is the Seebeck coefficient (also called the thermopower), $\rho$ is the resistivity, $\kappa_L$ and $\kappa_e$ are the lattice and electronic thermal conductivity, respectively. It is a very challenging task to increase the $ZT$ of a material since it is the combination of these three transport parameters $\alpha$, $\rho$, $\kappa$, which are correlated with each other. The resistivity and thermopower are strongly dependent on the carrier concentration. Therefore, compromises in manipulating these properties are unavoidable in order to increase material performance. At present, the current state-of-art TE materials are the traditional Bi$_2$Te$_3$, BiSb or their alloys, which are applicable for solid state cooling application at low temperature (T < 400K) and semiconducting SiGe.
alloy for power supply use at high temperature (T > 1000K). The maximum figure of merit for each of these materials is ZT ≈ 1 at their respective operating temperatures [1]. This current technological demands desire TE devices which exhibit performance efficiencies of around 20% which would require a material to have a ZT close to even larger than 2 or 3. The power factor, $a^2\sigma T$, (or $a^2T/p$) is typically optimized as a function of carrier concentration (typically around $10^{19}$ carriers/cm$^3$), through doping, to give the largest ZT. High mobility carriers are most desirable in order to have the highest electrical conductivity. Semiconductors have been primarily the materials of choice for potential thermoelectric applications, thus one would typically investigate covalently bonded systems of materials.

But, because of its high thermal and chemical stability and non-toxicity, ceramic oxide materials would be desirable for use at high temperatures for possible power generation applications. However, traditional TE theory would consider oxides possessing low mobility with primarily ionic bonding, thus possessing low electrical conductivity. Typically large mobility is thought to be an indispensable condition to make a good TE material. However, the appearance of a new transition-metal oxide, NaCo$_2$O$_4$ with unexpectedly favorable TE properties reported by Terasaki in 1997 challenges the traditional guiding principles about TE materials [2]. Single crystals of NaCo$_2$O$_4$ synthesized by NaCl flux method was found to be potential as a good p-type TE with low metallic in-plane resistivity, 0.2 mΩ·cm and large thermopower, 100 μV/K, although the mobility is quite low, 13 cm$^2$/V·s. The power factor ($a^2T/p$) of the NaCo$_2$O$_4$ single crystal exhibited a value of 1.5 W·m$^{-1}$·K$^{-1}$, which is even larger than that of Bi$_2$Te$_3$, 1.2 W·m$^{-1}$·K$^{-1}$ at 300K. After the discovery of this compound, other Co-based oxides, such as Ca-Co-O and Bi-Sr-Co-O systems, were also found to be good p-type TE materials [3,4,5,6,7]. In 2001, Fujita reported a ZT = 1.2 in a Na$_x$Co$_2$O$_4$ single crystal at 800K, comparable to traditional TE materials [8]. This high ZT value suggests these oxides are indeed promising p-type TE materials for potential high temperature use.

2. Crystal structure, synthesis and properties of Na$_x$Co$_2$O$_4$

Sodium cobalt oxide, as an intercalation compound with layered structure, belongs to the alkali ternary oxides group A$_2$MO$_2$ (A = Na, K; M = Co, Cr). It is sensitive to atmospheric moisture as first reported by Jansen and Hoppe in 1974 [9]. In 1980s, Delmas intensively investigated this oxide as a cathode material candidate due to its good electronic and electrochemical properties [10,11,12]. Stoichiometric NaCoO$_2$ is a semiconductor, but non-stoichiometric compound Na$_x$Co$_2$O$_4$ has a “metallic” character with good TE properties (x up to 1.5).

This ceramic oxide has a hexagonal layered structure with edge-sharing triangle CoO$_2$ sheets and Na layers alternately stacked along c-axis, i.e., sodium ions are intercalated between the two-dimensional CoO$_2$ sheets of octahedral, as shown in Figure 1 (where the Oxygen atoms are on the corners). Basically, Na$_x$Co$_2$O$_4$ is ionically bonded and belongs to space group P6$_3$22 with lattice constant of 2.8Å and c 10.8Å. Depending on the ratio of Na/Co, this material can exhibit four bronze type phases with different oxygen packing order and Na ions can be sandwiched between CoO$_2$ slabs in three different oxygen environments, trigonal prismatic, octahedral or tetrahedral [10].
In Na$_x$Co$_2$O$_4$, the CoO$_2$ sheet is conducting and strongly electron correlated which brings about the small metallic resistivity and enhanced thermopower. The Na layer, acting as the charge reservoir and donating electrons distributed among Co ions is insulating and highly disordered like an amorphous solid. The sodium atoms are thought randomly occupied part of positions in oxygen environment and the point-defect scattering leads to unexpected low thermal conductivity $\kappa \approx 2$ W-m$^{-1}$-K$^{-1}$ for polycrystalline NaCo$_2$O$_4$. Takahata considered this kind of sandwich structure consisting of crystalline metallic layers and the amorphous insulting layers advantageous to obtain good TE properties and he proposed this oxide is another example of Slack’s “PGEC” (phonon glass and electron crystal) materials [13].

Through modifying the NaCl flux method used by Terasaki via rotating the crucibles to increase the solution homogeneity and inserting a platinum wire with electricity into the surface of solution to reduce the nucleation, Mikami et al. obtained large plate-like crystals with sizes up to 10 x 10 x 0.5mm$^3$ [14]. Very recently, Peleckis et al. successfully grew Na$_x$Co$_2$O$_4$ whiskers with sizes up to 1.6 mm in length, 15-40 $\mu$m in width and 1.5-4.0 $\mu$m in thickness through an unconventional method from potassium-containing compositions [15]. The dried powders of Na$_2$CO$_3$, K$_2$CO$_3$ and Co$_3$O$_4$ were mixed and calcined at 750°C in air employing a “rapid heat-up” technique to avoid the evaporation of alkali metals. Calcined powders were pressed into pellets and sintered at 900°C for 12 hours. The whiskers were found to form at the partial-melt surface of the pellets. ICP-AES and EDX analyses indicated potassium was totally vaporized from the pellets and whiskers after firing. The values of thermopower $\alpha$, resistivity $\rho$ and power factor ($\alpha^2T/\rho$) of whiskers at 300K are 83 $\mu$V/K, 102 $\mu$Ω-cm and 2.1 W-m$^{-1}$-K$^{-1}$, respectively. The power factor of these single crystals is approximately 70% larger than that of Bi$_2$Te$_3$ compounds. Compared to the typical values of plate-like crystal by
NaCl-flux, the whisker crystals exhibit almost half of the resistivity value and larger power factor due most likely to its better quality and lower defect density. Based on the Boltzmann classic theory, if we assume the carrier concentration is $5 \times 10^{21}$ cm$^{-3}$, as previously reported, the estimated resistivity ($\rho = 1/\text{neu}$) for "perfect" crystal would be 0.1 m$\Omega$-cm. The experimental value of the resistivity of the whiskers is very close to the estimated value, which suggests that the whisker crystal is of high quality. One estimate of the impurity levels would be a measure of the residual resistivity ratio (RRR = $\rho_{\text{Q}} / \rho_{\text{DQ}}$), which however was not reported in this paper. Although from their graph, it appears to be on the order of 100. The author proposed the large amount of potassium evaporation could play a significant role in the whisker growth because it induced the partial melting of the pellets surfaces where the whiskers formed.

Due to the high structure anisotropy (insulating Na layer) and existence of grain boundaries, the $\rho$ of polycrystalline Na$_x$Co$_2$O$_4$ samples obtained by traditional solid state reaction is ten times higher than single crystal, and as a result, the power factor $\alpha^2 T / \rho$ is much smaller. The value of $Z (-10^{-4} \text{K}^{-1})$ of polycrystalline sample is much smaller than traditional TE semiconductors, but it’s the highest among the polycrystalline oxides. Since Na is volatile, the manner in which to control the composition is a challenging aspect of the material synthesis, and the typical way is adding excess sodium in the starting materials to compensate the loss during the firing [16]. Motohashi, etc. developed a new technique “rapid heat-up” to precisely control the Na content by avoiding Na evaporation [17]. It was found with increasing $x$ (Na content), $\rho$ decreased and $\alpha$ increased simultaneously, which appeared to be incompatible with the conventional band structure. For the $x = 1.5$ sample, $\alpha$ reached an unusual high value of 120 $\mu$V/K with small $\rho$ of 3.0 m$\Omega$-cm at 300K. This Na-rich compound Na$_{1.5}$Co$_2$O$_4$ was detected to possess an unconventional 2nd order magnetic transition at 22K where an apparent jump in specific heat, an onset of extremely small spontaneous magnetization and a kink in the resistivity showed up [18]. Zero-field $\mu$SR measurement found the existence of internal magnetic field at temperature below 22K ($T_m$) in a polycrystalline Na$_{1.5}$Co$_2$O$_4$ sample by muon-spin-rotation and relaxation spectroscopy [19]. Ohtaki, and his collaborators used double-step sintering to get high thermopower values $\alpha \approx 190$ $\mu$V/K and $ZT \approx 0.78$ at 800°C [20]. Tajima, et al. employed reactive template grain growth (RTGG) to obtain highly textured ceramic with high a power factor 0.2- 0.5 W-m$^{-1}$K$^{-1}$ at 1000K [21]. Nagai, et al. prepared high-quality polycrystalline samples with high $ZT$ value of 0.8 at 1000K by a polymer-conjugation technique [22]. Doping is an effective way to tune up the properties of ceramic oxides, as alloying to metals. Terasaki studied the doping effects of both Na-site and Co-site, and found partial substitution of Cu with Co can enhance $\alpha$ and $ZT$ [16,23,24,25].

3. Role of Co ions and strongly correlated electron behavior

Na$_x$Co$_2$O$_4$ exhibits a small metallic resistivity due to it large carrier concentration, but its thermopower is much larger than that of a typical metal or semimetal. The spin state of Co ions and strong electron correlation in CoO$_2$ sheet are thought to strongly contribute to the enhanced thermopower. In NaCo$_2$O$_4$, the Co ions with outer valence electron configuration 3d$^7$4s$^2$ have the charge of +3.5. $^{59}$Co NMR study along with susceptibility results revealed there exist two distinct Co ions at low spin states, i.e.,
nonmagnetic Co$^{3+}$ with spin $s = 0$ and magnetic Co$^{4+}$ with $s = 1/2$ [26]. The Co ions do not behave equally like Co$^{3+}$. Due to the octahedral O environment, the 3d electron of Co ions are crystal field split into two distinct energy levels, upper-lying two-fold level $e_g$ where wavefunctions point toward O$^{2-}$ ions ($d_{x^2-y^2}, d_{3z^2-R^2}$) and lower-lying three-fold level $t_{2g}$ where wavefunctions point between O$^{2-}$ ions ($d_{xy}, d_{yz}, d_{zx}$), separated by approximately 2.5 eV [27]. The $t_{2g}$ width is 1.6eV and $e_g$ bandwidth is 1.2 eV. $E_F$ is in the top of $t_{2g}$ manifold, 0.22eV below the band edge. There is 0.5 hole per Co ion and 1 hole per unit cell (2 Co ions). The elementary charge-transport process is the hopping of a hole from the Co$^{4+}$ site to Co$^{3+}$ site, as shown in fig. 2 [28].

Fig. 2 Co ions 3d orbitals

Like other transition-metal oxides, Na$_x$Co$_2$O$_4$ is also an electron-correlated system, where electrons are localized at atomic sites and lose their mobility due to the strong Coulombic repulsion. For example, the d electrons in transition metal ions, experience the competing forces: electron interaction tends to localize electrons at lattice sites, while the hybridization with the oxygen p electron states tends to delocalize the electrons [29]. The competition between the crystal field splitting and Hund’s coupling determines the spin and orbital states of Co ions.

The evidence of strong electron correlation that exists in this oxide could be as follows:

1. Bandwidth W ($t_{2g}$ is around 1.6 eV) is much smaller than Coulomb on-site repulsion $U$. Though there are no detailed photoemission studies done to get the $U$ yet, but from other octahedrally coordinated 3d transition metal compound, we can estimate the effective on-site Hubbard $U$ around 5-8 eV [27].

2. Much larger electronic specific heat coefficient $\gamma$, 48 mJ/mol-K$^2$ of (Na,Ca)Co$_2$O$_4$ than ordinary metals, such as Cu - 6 mJ/mol-K$^2$ [30]. The strong correlation bringing about the large $\gamma$ was thought to be from low dimensionality and frustrated spin structure of triangle CoO$_2$ sheets.

3. The resistivity of NaCo$_2$O$_4$ continues to decrease down to low temperature 4.2K, where no phonons are thermally excited [31]. For ordinary metals, at very low temperature where there is no electron-phonon scattering, resistivity is constant due to
the scattering from impurities or point defects. The continuing decrease of resistivity of NaCo$_2$O$_4$ at low temperature could be from electron-electron scattering.

4. The source of enhanced thermopower and the estimation of high T limit

As mentioned previously, the thermopower of metallic Na$_x$Co$_2$O$_4$ is much higher than ordinary metals. Extensive work has been performed to reveal the origin of the enhanced thermopower. Terasaki and his collaborators proposed it could arise from the spin fluctuation, similar to heavy fermions and/or valence-fluctuation systems [2]. They estimated the effective mass ($m^*$) and found it was two orders of magnitude higher than $m^*$ of copper-based High temperature superconductors (HTSC). Hall effect experiments indicate this oxide shows large negative magnetoresistance and a very small Hall coefficient [31]. Ando et al. measured the specific heat of (Na, Ca)Co$_2$O$_4$ and found it had large electron specific-heat coefficient $\gamma$ [30]. However, these investigations did not reveal the issue of the enhanced thermopower.

Recently, researchers from Princeton University showed experimentally that the large $\alpha$ comes from the electronic spin entropy, which is believed to dominate the entropy current [28]. In the electron correlated system, the spin degrees are predicted to produce a large contribution to $\alpha$ as the Heikes formula $\alpha = -\sigma / e = -K_s (\ln g_s + \ln g_x) / e$. The spins are not fixed to specific atoms within the lattice, instead are free to move around. Therefore, if the applied magnetic field is strong enough to remove the spin degeneracy ($g_s = 1$), thermopower should vanish to zero, only if the spin entropy really provides the main contribution. That’s exactly what they found in their experiment.

As shown in their paper, the in-plane thermopower is strongly suppressed at low temperature with the application of a longitudinal (in-plane) or transverse (c-axis) magnetic field, [28]. Since the in-plane field only couples the freedom of spin, but not to the orbital degrees, the observed suppression is only due to the spin degeneracy lifted by the field. This doesn’t occur in an ordinary metal, because the spins are tied to delocalized electrons. In Na$_x$Co$_2$O$_4$, the strong electron on-site repulsion excludes double occupancy of a site by holes, and the elementary charge-transport process is the hole hopping from Co$^{4+}$ (s=1/2) to Co$^{3+}$ (s=0). During this process, we also can transfer a spin -1/2 along with the hole, which means a transfer of spin entropy, $\sigma = k_B \ln 2$. The moving spins carrying energy, call spin entropy are thought behind the enhanced thermopower. It’s found that the spin entropy term accounts for almost all of thermopower $Q$ at 2K and 2/3 at 300K.

From narrow-band Hubbard model, we can predict the effect of electron correlation to the thermopower. The high temperature limit (thermal energy $k_B T$ is much larger than transfer integral/energy $t$) of thermopower $\alpha$ can be given by [32,33]:

$$\alpha = \frac{1}{eT^2} \frac{1}{\mu} = \frac{\mu}{eT} = \frac{1}{e} \frac{\partial \sigma}{\partial N} = -\frac{K_s}{e} \frac{\partial \ln g}{\partial N}$$
Here $\mu$ is chemical potential, $\sigma$ is entropy of system and $g$ is degeneracy or configuration and $k_B$ is the Boltzman constant. In the strong electron interaction (on-site Columbic repulsion $U$) system $\text{Na}_x\text{Co}_2\text{O}_4$, for the high $T$ limit case, $t \ll k_B T \ll U$, the configuration with doubly occupied sites is excluded. The total number of possible states of system $g$ can be expressed as:

$$g = g_3 \mu g_4^M N_A ! \over M ! (N_A - M) !$$

Here $g_3$ and $g_4$ are the degeneracies (number of configurations) of $\text{Co}^{3+}$ and $\text{Co}^{4+}$ ions at a certain spin state respectively, $N_A$ and $M$ are the total number of sites and $\text{Co}^{4+}$ site, respectively. Koshiba deduced the following equation to estimate the high temperature limit of thermopower as a function of $g_3$ and $g_4$ [32]:

$$\alpha = -k_B \ln(g_3 \over g_4)$$

Where $y (= M/N_A)$ and $1-y$ are the concentration of $\text{Co}^{4+}$ and $\text{Co}^{3+}$ ions, respectively. Table 1 summarized the ratio of $g_3$ and $g_4$ and the estimated high $T$ limit of thermopower. But in $\text{Na}_x\text{Co}_2\text{O}_4$, the competition between the Hund’s coupling and crystal field splitting force determine the $\text{Co}^{3+}$ and $\text{Co}^{4+}$ are in low spin state. Therefore, the high $T$ limit for $\text{NaCo}_2\text{O}_4$ ($y = 0.5$) and $\text{Na}_{1.5}\text{Co}_2\text{O}_4$ ($y = 0.25$) are $154 \mu\text{V/K}$ and $227 \mu\text{V/K}$ respectively. This calculation may explain the seemingly contradictive phenomenon that the thermopower increases and the resistivity decreases simultaneously with increasing Na concentration [17]. The possible reason could be the increase of the carrier concentration leads to a decrease in the resistivity and a change of ratio $g_3/g_4$ results in the enhancement of the thermopower.

<table>
<thead>
<tr>
<th>Cases</th>
<th>$\text{Co}^{3+}$ site</th>
<th>$\text{Co}^{4+}$ site</th>
<th>ratio $g_3/g_4$</th>
<th>$\alpha$ ($\mu\text{V/K}$) for $\text{NaCo}_2\text{O}_4$ ($y=0.5$)</th>
<th>$\alpha$ ($\mu\text{V/K}$) for $\text{Na}_{1.5}\text{Co}_2\text{O}_4$ ($y=0.25$)</th>
</tr>
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<tbody>
<tr>
<td>I</td>
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<td>HS</td>
<td>15/6</td>
<td>-79</td>
<td>16</td>
</tr>
<tr>
<td>II</td>
<td>HS+LS</td>
<td>HS</td>
<td>16/6</td>
<td>-84</td>
<td>10</td>
</tr>
<tr>
<td>III</td>
<td>LS</td>
<td>HS+LS</td>
<td>1/12</td>
<td>214</td>
<td>309</td>
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<tr>
<td>IV</td>
<td>LS ($s=0$)</td>
<td>LS ($s=1/2$)</td>
<td>1/6</td>
<td>154</td>
<td>227</td>
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<tr>
<td>V</td>
<td>HS+LS+IS</td>
<td>HS+LS+IS</td>
<td>34/36</td>
<td>5</td>
<td>79</td>
</tr>
</tbody>
</table>

* HS: high spin state; IS: intermediate spin state; LS: low spin state.

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5. Superconductivity in Na$_x$Co$_2$O$_4$·yH$_2$O

Recently, Takada first reported the surprising superconducting behavior under 5K in the hydrated form of this oxide Na$_x$Co$_2$O$_4$·yH$_2$O, this new discovery may give people valuable clues to the mechanisms of superconductivity in the cuprates. After Takada et al. reported the superconductivity behavior (T$_c$~5K) in the hydrated form of sodium cobalt oxide[34]; more attention has been attracted to this system of materials as an interesting physical system. Through a chemical oxidation process, the hydrated form Na$_x$Co$_2$O$_4$·yH$_2$O sample was obtained from a parent compound Na$_{4.4}$Co$_2$O$_4$. Water was intercalated into the bulk structure between the layers of CoO$_2$ and Na, as shown in fig. 4(a). ICP-AES analysis determined x = 0.70 and y = 2.6. The sudden drop to negative of magnetic susceptibility just below 5K was clearly observed. Such a strong diamagnetism, due to the expulsion of magnetic flux by a supercurrent, is a significant signal of the onset of superconductivity. The sharp decrease of resistivity observed at around 4K also supports the superconducting transition. The thick insulating layer of water which is intercalated between the CoO$_2$ sheet and Na layer was thought to play an essential role to induce superconductivity.

Recently Cava and his colleagues found T$_c$ varied with Na content x and reached its highest value 5K near x = 0.6 [35]. Although the T$_c$ of this material is far below 100K or most of copper oxides, the mechanism behind it may give us some valuable hint to understand the source of superconductivity in the cuprates because of their resemblance in structure, such as 2D character of CoO$_2$ layer and CuO$_2$. The main difference between these two layered oxide systems is that the Co ions form the triangle lattice with spins frustrated geometry, but CuO$_2$ plane forms the square lattice of antiferromagnetic spins. Fujii and Terasaki recently proposed a “block-layer” concept for the layered Co oxides, as is established in HTSC [36]. For superconducting Na$_x$Co$_2$O$_4$·yH$_2$O, Kobayashi et al. reported the T dependence of the Knight shift K$_y$ from $^{59}$Co NMR study [37]. The existence of the coherence peak in the spin-lattice-relaxation-rate versus T indicates this superconducting compound has the spin singlet pairs with s-wave symmetry. $^{59}$Co NQR study also shows this hydrated oxide is a fully gapped superconductor and the superconductivity is thought to take place close to a ferromagnetic phase [38].

6. Some of Our Recent Results:

In our lab, the polycrystalline Na$_x$Co$_2$O$_4$ samples were synthesized by traditional solid-state reaction. Starting materials, Na$_2$CO$_3$ and Co$_3$O$_4$ powders were mixed and ground, then calcined in air at 800-860°C for 12 hours. After finely ground, the calcined powders passed through three screens with pore sizes of 80, 200 and 325 mesh. Then the cold-pressed pellets were sintered as stacked pieces in air at 900 - 950°C for 12 hours. 20% excess of sodium was added in the starting materials to compensate the loss of Na during the firing. The results showed the calcination and sintering temperatures do not greatly affect TE properties of polycrystalline samples, but it’s apparent that the sintered pieces from the calcined powders which passed through 325 mesh screen always exhibit relative larger thermopower along with higher resistivity, compared to the pellets prepared from powders which passed through 80 mesh and 200mesh sieves. The transport properties, including thermopower, resistivity and thermal conductivity, were measured using the systems, which are self built-up in our lab. The Dupont silver
paint 4922N was applied for the electric contact. The details about the measuring systems were described in somewhere else [39,40]. All the samples have relatively good reproducibility in the properties.

As shown in Figure 3, the polycrystalline Na$_x$Co$_2$O$_4$ samples have the values of thermopower $\alpha \approx 83 \, \mu \text{V/K}$, $\rho \approx 1.75 \, \text{m}\Omega\text{-cm}$ and $\kappa \approx 2.0 \, \text{W/m-K}$ at 300K. The power factor $\alpha^2 T/\rho$ and ZT are shown in Figure 4, equal to 0.12 and 0.06 at 300K, respectively. The estimated electronic thermal conductivity from the W-F law is less than 10% of total thermal conductivity, which gives us some hope to further reduce the thermal conductivity by introducing extra phonon scattering mechanisms, such as impurities and grain boundaries, and possible point defect scattering from the disordered and randomly position-occupied Na atoms. Of course, since the thermopower, resistivity and thermal conductivity are correlated, reduction in thermal conductivity by introducing additional scattering centers may unavoidably lead to an undesired effect on the thermopower and resistivity. The tendency of ZT increase with increasing temperature show this oxide may be applicable for high temperature use for power generation.

![Fig. 3 Transport data of polycrystalline Na$_x$Co$_2$O$_4$](image)

![Fig. 4 Power factor $\alpha^2/\rho$ and ZT](image)
The SEM microstructure of thermally etched top surface and fracture surface of sintered samples is shown in Figure 5. The grains are not very homogeneous in size and shape; the average size is around 10 μm. From the fracture surface, the apparent intergranular fracture and existence of large amount of pores suggested the low bulk density of the polycrystalline samples after sintering, which is in agreement with the calculated relative density (< 80%). Kurosaki et al. reported the density of hot-pressed samples was also as low as 84% [41], much smaller than the high density (> 99%) of typical hot-pressed ceramic oxides, such as transport PLZT.

Single crystals Na$_x$Co$_2$O$_4$ were synthesized by NaCl flux method. Crystals were grown from the melt when it’s cooled down from 950°C to 850°C with slow cooling rate 0.3-0.6 °C/hr. The typical size of single crystals is ~ 0.5-2 mm x 0.5-2 mm x 10-50 μm. The hexagonal plate-like crystal, as shown in Figure 6(a), reflects the hexagonal layered structure of this oxide. The XRD spectra shown in Figure 6(b) also indicates that the crystal is c-axis inclined. Only singe phase (γ phase) is observed for both single crystal and polycrystal, except a few weak peaks from unreacted Co$_2$O$_4$. As displayed in Figure 7 the thermopower of a single crystal is measured to be around 100 μV/K and the in-plane resistivity $\rho \sim 0.30$ mΩ-cm. The in-plane resistivity below 100K exhibits a very linear temperature dependence, to quite low temperatures, and is indicative of the electron correlation in this system. The value of power factor $\sim$0.3 W-m$^{-1}$K$^{-1}$ at 300K is almost 10 times larger than that of the polycrystal form due to the high anisotropy in resistivity ($\rho_\parallel \ll \rho_\perp$) derived from the layered structure with alternately stacked conducting CoO$_2$ sheet and insulating Na layer.

Magnetic properties of Na$_x$Co$_2$O$_4$ samples were measured by SQUID system with field of 0.5T. The magnetic susceptibility $\chi$ is surprising high, as shown in fig. 10(a). Cava found at 2K, that $\chi$ is almost two orders of magnitudes higher than that of ordinary metals [42]. The temperature dependence of susceptibility can be fit by Curie - Weiss
law $\chi = \chi_0 + C/(T-\theta)$, we can obtain Curie constant $C = 0.29$, $\chi_0 = 5 \times 10^{-4}$ emu.mol$^{-1}$ and Curie temperature $\theta = -80$K. This close fit tells us there exist some localized magnetic moments in the material, which is in agreement with the static magnetic order observed in Na-rich compound Na$_{1.5}$Co$_2$O$_4$ [19]. Also it explains why this material possess high $\chi$, since $\chi$ is the ease with a magnetic field can align the spins. The magnetic moment is calculated by the equation $\mu_{\text{eff}} = 2.84(\chi_m T)^{1/2}$ and found it's around 1.74$\mu_B$, close to the theoretical value of 1.73$\mu_B$. As shown in Figure 8(b), the powders ground from the sintered sample possess a little bit smaller magnetic moment than the calcined powders. This result is opposite to what one would expect, the ratio of Co$^{4+}$/Co$^{3+}$ should increase due to the small amount loss of sodium in sintering and Co$^{4+}$ ions with spin 1/2 is magnetic but Co$^{3+}$ with zero spin is non-magnetic, so magnetic moment should increase slightly. The reason could be the inhomogeneous distribution of composition or the
impartment of incipient localized spin moment due to the grinding to the sintered pellets.

Fig. 8 (a) magnetic susceptibility $\chi$ 
(b) Magnetic moment $\mu_{\text{eff}}$

7. Future research directions

As pointed out previously, the $\text{Na}_x\text{Co}_2\text{O}_4$ material possesses very low thermal conductivity $\kappa \sim 2 \text{ W-m}^{-1}\text{K}^{-1}$ due to the disordered sodium atoms behaving like glass. Typical materials with light atoms such as oxygen have high $\kappa$, for example high temperature superconducting copper oxides have $\kappa$ around 4-5 $\text{W-m}^{-1}\text{K}^{-1}$. Up to now, very few papers have given a theoretically detailed analysis about how the Na deficiency brings about the low $\kappa$ by reducing the phonon mean free path as a result of point defect scattering. In this system, electronic thermal conductivity is only a very small portion of total thermal conductivity; so it is possible to further decrease the thermal conductivity by introducing additional phonon scattering mechanisms, such as impurities and grain boundaries. Theoretical calculations are needed to predict the lowest limit of $\kappa$ that the compound may achieve. Systematic studies concerning the impact of Na-site doping and Na content on $\kappa$ is also lacking.

Without high-quality samples, it's impossible to get definitive results. Currently it is still challenging work to get large single crystals or textured polycrystalline $\text{Na}_x\text{Co}_2\text{O}_4$ with high quality for properties characterization. Successful growth of $\text{Na}_x\text{Co}_2\text{O}_4$ whiskers may give us some useful hint to develop a new approach for single crystal synthesis although the whisker growth mechanism is not clear yet.

Based on Koshibae’s calculation, $\text{Na}_x\text{Co}_2\text{O}_4$ with high spin states of Co$^{3+}$ and Co$^{4+}$ ions can be a n-type TE material. At present, the typical n-type TE oxides are Al-ZnO [43,44], Ca-Mn-O [45] and Ba-Pb-O [46] systems. Due to their isotropic structures, properties of single crystals are not superior to polycrystalline samples. No n-type oxide has been discovered which possesses TE properties comparable to Co-based p-type crystals, although polycrystalline samples of the present n-type oxides and Co-
based p-type oxides have close ZT values. If there is a feasible way to synthesize the n-type Na$_x$Co$_2$O$_4$ TE crystal, its properties arising from the superior layered structure will be better than any of the present n-type oxides. However, how to control the spin states of Co ions is definitely a problem, by firing environment or doping? All the dopants, which have been currently investigated, only deteriorated the properties (except Cu), and have not changed the sign of thermopower [23,24,25]. But with the emergence of new materials synthesis technology, we may discover a way to make n-type Na$_x$Co$_2$O$_4$ with good properties.

As a new group of TE materials, the intriguing electronic and magnetic properties of Na$_x$Co$_2$O$_4$ associated with the layered structure, such as the enhanced thermopower [28], superconductivity in Na$_x$Co$_2$O$_4$·H$_2$O [34], static magnetic field [19] and 2nd order magnetic transition [18] in Na$_{1.5}$Co$_2$O$_4$ are the spotlights of future studies. The electron correlation, spin-entropy and the structure frustration arising from triangle CoO$_2$ sheet are thought to be the key ingredient for the good TE properties. But compared to other transition metals, such as LiVO$_3$, less progress has been made to Na$_x$Co$_2$O$_4$. For example, what do the orbital-spin patterns look like and where is the enhanced effective mass from are still not clear and electron repulsion U has not been calculated yet. But one thing has made clear, the superior hexagonal layered structure with conducting and electron correlated CoO$_2$ sheet and insulating Na layer makes this transition-metal oxide, Na$_x$Co$_2$O$_4$ a promising TE material.

Acknowledgements

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TRANSPORT AND OPTICAL PROPERTIES OF THE TYPE II CLATHRATES 
Cs$_8$Na$_{16}$Si$_{136}$ AND Si$_{136}$

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ABSTRACT

In recent years there has been a thrust in interest on novel open structured materials. Many of these materials are characterized by their ability to host guest atoms in interstitial “voids,” giving rise to a range of interesting physical properties. In particular, compounds with crystal structures isomorphous to the type I and II clathrate hydrates are being studied due to their potential for use as thermoelectric materials. Of the two polymorphs the type II clathrates have been investigated less extensively, both theoretically and experimentally. In this paper we present an overview of the temperature dependent electrical and thermal transport properties as well as Raman scattering spectra for the type II clathrates Cs$_8$Na$_{16}$Si$_{136}$ and Si$_{136}$. Prospects for applications and future directions are also discussed.

INTRODUCTION

The class of materials collectively referred to as clathrates are currently under investigation due to the unique properties they possess, in addition to their potential for various applications. The unique structure-property relationship found in these materials forms the impetus for understanding their transport properties. The interest for possible applications includes superconductivity (1), opto-electronics (2, 3), and thermoelectrics (4).

The efficiency of a thermoelectric material is determined by the dimensionless figure of merit $ZT$,

$$ZT = \frac{S^2 \sigma }{K} T . \quad [1]$$
Here $T$ is the absolute temperature, $S$ is the Seebeck coefficient, $\sigma$ is the electrical conductivity, and $\kappa = \kappa_e + \kappa_l$ is the thermal conductivity, consisting of electronic ($\kappa_e$) and lattice ($\kappa_l$) contributions. Simply put, the larger the $ZT$, the better the thermoelectric performance. From this simple expression, the desired properties for a good thermoelectric material are apparent: the electrical properties must be good and the thermal conductivity low. However, the material parameters present in Eq. [1] are not all independent, thus maximizing this expression proves to be a formidable task. For the better part of the past 50 years, the approach to thermoelectric materials design has not changed appreciably, drawing upon the work of Ioffe (5). This approach has been to construct binary semiconducting compounds of heavy elements from the lower part of the periodic table, resulting in the Bi, PdTe, and Bi$_2$Te$_3$ systems currently used as thermoelectrics. Since their establishment, the room temperature $ZT$ of conventional materials has remained near 1, which has limited thermoelectrics to specialized and “niche” applications. There appears no theoretical reason why a $ZT$ of 3 or 4 cannot be attained, which would result in thermoelectric technology being competitive with compressor based cooling devices (6).

Recently, several new approaches to the search for new thermoelectric materials have been suggested and pursued (7, 8). In particular, Slack has proposed that certain open-structured semiconductors that can incorporate atoms inside crystallographic voids may have favorable thermoelectric properties (9). At the core of this idea is that these encapsulated atoms (typically metals) may resonantly scatter the heat carrying acoustic phonons through localized vibrations inside their atomic “cages” without adversely affecting the electron transport. Various studies of type I clathrates have shown that this approach is effective (4). For example, in their studies of the type I clathrate Sr$_9$Ga$_{16}$Ge$_{30}$ Nolas et al. measured a relatively high electron mobility in crystalline semiconductors that exhibited a “glass-like” thermal conductivity (10). A $ZT$ value above 700 K approaches 1, and compares favorably with conventional PbTe materials at these temperatures. The type I clathrates have been studied quite extensively, but less investigated have been the type II clathrates. We now discuss the characteristics of both type I and II clathrates, along with some of the mechanisms for the physical properties of these materials.

CRYSTAL STRUCTURE AND PROPERTIES

The unique crystal structure of clathrates directly determines many of their interesting properties. Of the large number of compounds collectively known as clathrates, two structures in particular have raised interest for potential use as thermoelectrics. Referred to as type I and type II, these compounds crystallize in the corresponding clathrate hydrate crystal structures. In the ice clathrates, the framework of the crystal structure consists of tetrahedrally coordinated, hydrogen bonded H$_2$O molecules arranged in a zeolite-like structure. The framework can then encapsulate atoms or molecules, such as Xenon or methane. In the 1960’s Kasper et al. (11) and Cros et al. (12) synthesized and determined the structure of the Group IV analogues to the clathrate hydrates, in which the
framework consists of covalent $sp^3$ bonded Si atoms encapsulating Na ions (see Fig. 1b and 2b).

The type I clathrates form with the space group $Pm\bar{3}n$, and can be represented by the formula unit $M_8E_{46}$. Here $M$ is typically an alkali or alkaline earth metal, and $E$ represents one of the Group IV elements silicon, germanium, or tin. Substitutions are possible on the $E$ site, as in the case of $Sr_8Ga_{16}Ge_{30}$. The type I unit cell is formed by two pentagonal dodecahedra and six tetrakaidecahedra (coordination number $CN = 20, 24$, respectively; see Fig. 1a) that share faces of five and six member rings to form the crystal structure (Fig. 1b). The framework is formed by the covalently bonded $E$ atoms, which are tetrahedrally coordinated by other $E$ atoms and reside at the vertices of the polyhedra. The $M$ atoms are found inside the polyhedra, and are weakly bonded to the framework. This is the most interesting aspect of these materials, since the $M$ atoms may “rattle” inside their atomic “cages,” creating strong phonon scattering centers. The frequencies of vibration of the metal atoms are typically low, so that they may resonantly scatter the heat carrying acoustic phonons in these materials. This can result in a low lattice thermal conductivity for the clathrate, and has been shown to be the case in various studies of type I clathrates (10, 13, 14), in particular with $Sr_8Ga_{16}Ge_{30}$ as noted above. The room temperature value for the thermal conductivity of this crystalline material is lower than that of amorphous $SiO_2$. In addition to this, the thermal conductivity of $Sr_8Ga_{16}Ge_{30}$ was found to have a $T^2$ temperature dependence at low temperatures, which is typical of amorphous materials. Numerous studies, both theoretical and experimental, corroborate the idea that the filler atom resonantly scatters phonons, and that this is a dominant mechanism for the low thermal conductivity in this material (4, 15, 16, 17, 18).

![Figure 1](image.png)

**Fig. 1.** (a) The polyhedra that form the type I clathrate crystal structure. (b) A depiction of the conventional unit cell of the type I clathrate, with encapsulated atoms shown inside two of the polyhedra (bold).
Fig. 2. (a) The polyhedra that form the type II clathrate crystal structure. (b) A depiction of the conventional unit cell of the type II clathrate, with encapsulated atoms shown inside two of the polyhedra (bold).

The type II clathrates crystallize with the space group $Fd\bar{3}m$, and can be represented by the formula unit $M_xE_{136}$ (typically $M =$ alkali/alkaline earth, $0 < x < 24; E =$ Si, Ge). Many of the basic structural characteristics of the type II clathrates are the same as for the type I, but in case of the type II clathrates it is sixteen dodecahedra and eight hexakaidecahedra (CN = 20, 28, respectively; see Fig. 2a) that share faces to construct the conventional unit cell (Fig. 2b). Another significant difference between the two types is that in the case of the type II clathrates, specimens may be synthesized that have a fractional filling, as seen in the formula $M_xE_{136}$. Here $x$ can vary from zero, as is the case in Si$_{136}$ where essentially all of the voids are empty, to a full stoichiometric filling of the voids in which essentially each site is occupied ($x = 24$), as in the case of Cs$_6$Na$_{16}$Si$_{136}$ (here there are two different filler atoms: Cs in the larger hexakaidecahedra, Na in the smaller dodecahedra). The ability to fractionally fill the type II clathrates has a direct effect on the properties of these materials, and is an aspect that warrants further investigation.

RESULTS AND DISCUSSION

Detailed explanations of the synthesis of Cs$_6$Na$_{16}$Si$_{136}$ and Si$_{136}$ can be found in references (19) and (3), respectively. There has only been a small number of type II Group IV clathrates synthesized. They remain of interest for future study. The synthesis of the unfilled type II clathrate Si$_{136}$ was a significant result since this material constitutes
a new, previously unknown stable phase of elemental Si, the most important semiconductor (3). The synthesis of Si$_{136}$ also proved unequivocally that the framework of the type II silicon clathrate is stable upon removing the filler atoms from their voids. Some of the various physical properties of Cs$_6$Na$_{16}$Si$_{136}$ and Si$_{136}$ are presented below.

**Transport Properties**

The electrical properties of polycrystalline Cs$_6$Na$_{16}$Si$_{136}$ and Si$_{136}$ have been studied by Nolas et al. (19) and Gryko et al. (3), respectively. As shown in Fig. 3, the resistivity for Cs$_6$Na$_{16}$Si$_{136}$ shows an increase with temperature, typical of metallic behavior. The sign of the Seebeck coefficient indicates that electrons are the majority carriers, and the relatively small value for the Seebeck coefficient is also consistent with metallic behavior. The resistivity values are relatively high, possibly due to a residual resistivity attributed to impurities at the grain boundaries of the polycrystalline sample (19). Metallic behavior has been observed in other studies of stoichiometric type I and II clathrates (20, 21), and is attributed to the alkali atoms donating electrons to the framework conduction bands.

![Graph showing resistivity and Seebeck coefficient vs. temperature](image)

**Fig. 3.** Electrical resistivity (filled circles) and Seebeck coefficient (open squares) of Cs$_6$Na$_{16}$Si$_{136}$. Both properties indicate metallic behavior for this material.
Theoretical calculations predicted that the elemental clathrate $\text{Si}_{136}$ is a semiconductor with an indirect band gap of $\approx 1.9$ eV (2). Gryko et al. in their initial work on $\text{Si}_{136}$ measured the temperature dependence of the resistance and performed optical absorption measurements (3). From Arrhenius plots of the resistance and the optical measurements, it was found that the intrinsic band gap is $1.9-2.0$ eV, in good agreement with theory. This band gap is approaching twice the value for the familiar diamond-structured silicon, which has an intrinsic band gap of $1.1$ eV.

The thermal conductivity of $\text{Cs}_8\text{Na}_{16}\text{Si}_{136}$ and $\text{Si}_{136}$ was measured by Nolas et al. (19, 22) and is presented in Fig. 4. We see that the thermal conductivity of $\text{Cs}_8\text{Na}_{16}\text{Si}_{136}$ is relatively large, as compared to type I clathrates such as $\text{Sr}_2\text{Ga}_{16}\text{Ge}_{30}$ (10). This can be attributed to the electronic contribution to the thermal conductivity of the former material. Note the thermal conductivity of $\text{Si}_{136}$ in Fig. 4. This material has a very low thermal conductivity for a guest-free clathrate; at room temperature the value is thirty times lower than diamond-structured silicon. Filler atoms are not present in $\text{Si}_{136}$ to resonantly scatter the heat carrying acoustic phonons, so other mechanisms must be the

![Graph](image)

**Fig. 4.** Thermal conductivity of $\text{Cs}_8\text{Na}_{16}\text{Si}_{136}$ (open circles) and $\text{Si}_{136}$ (closed circles). The thermal conductivity for $\text{Cs}_8\text{Na}_{16}\text{Si}_{136}$ is relatively high, and can be attributed to the electronic contribution to the thermal conduction in this material. The thermal conductivity for $\text{Si}_{136}$ is very low; at room temperature, thirty times lower than diamond structured silicon. Note the $T^3$ dependence at lower temperatures.
cause. We speculate that the increased number of atoms per unit cell as compared to diamond-structured silicon may be a cause of the decrease in thermal conductivity, with the possibility of optical phonons participating in the thermal conduction.

**Optical Properties**

Fig. 5 shows room temperature Stokes Raman spectra for the (a) Si$_{136}$ and (b) Cs$_8$Na$_{16}$Si$_{136}$ specimens in parallel (VV) and perpendicular (HV) polarizations of the incident and collected light (23). The framework Raman modes of Cs$_8$Na$_{16}$Si$_{136}$ resemble...
those of Si$_{136}$. Experimentally, the higher frequency silicon framework modes (above 300 cm$^{-1}$) of Cs$_8$Na$_{16}$Si$_{136}$ are shifted towards lower frequency as compared to those of Si$_{136}$, as predicted by theoretical calculations (23). The framework modes below 300 cm$^{-1}$ remain relatively unperturbed, indicating that the metal-framework interaction has a stronger effect on the higher frequency optic modes. Physically, the higher frequency modes tend to originate from bond stretches between a pair of Si framework atoms. The "guest-free" Si$_{136}$ material is a semiconductor, while Cs$_8$Na$_{16}$Si$_{136}$ is a metal. Assuming a rigid band model, the additional electrons from Cs and Na are donated to the framework conduction bands. These bands are primarily anti-bonding states; occupying these reduces the Si-Si bond order to a value less than that of a single bond. This diminishes the restoring stretch force and reduces the frequency.

The localized "rattle" modes of Cs inside the hexakaidecahedra were identified at 57 cm$^{-1}$ for Cs$_8$Na$_{16}$Si$_{136}$. This mode is in the range of the acoustic phonons in this crystal structure. The localized phonon-scattering centers created by the dynamic disorder of the Cs atoms encapsulated in their atomic "cages" may resonantly scatter the framework acoustic phonons and result in low thermal conductivities in semiconducting variants.

**CONCLUSIONS AND FUTURE DIRECTIONS**

Clathrates are a class of materials so named for their "open" crystal structure and the ability to host guest atoms inside crystallographic voids. In particular, the semiconducting variants of these materials are of interest due to their favorable electrical properties and "glass-like" thermal conductivity, which result in promising thermoelectric properties. Of the two types currently being investigated with thermoelectrics in mind, the type II have been less studied.

In this paper, we have presented an overview of some of the various properties of the type II clathrates Cs$_8$Na$_{16}$Si$_{136}$ and Si$_{136}$. The electrical properties show Cs$_8$Na$_{16}$Si$_{136}$ to be metallic and Si$_{136}$ to be semiconducting with a wide indirect band gap of approximately 2.0 eV. The thermal conductivity of Cs$_8$Na$_{16}$Si$_{136}$ is larger than that of type I clathrates such as Sr$_8$Ga$_{16}$Ge$_{26}$ due to the electronic contribution in this material. However, the thermal conductivity of Si$_{136}$ is very low for a guest-free clathrate: thirty times lower than for diamond-structured silicon at room temperature. In order to fully understand the vibrational properties in these materials, most of the Raman active modes for both clathrates have been identified. The metallic behavior of Cs$_8$Na$_{16}$Si$_{136}$ excludes this material from being a useful thermoelectric in its present form, but semiconducting variants of stoichiometric type II clathrates may have favorable thermoelectric properties. The semiconducting behavior and remarkably low thermal conductivity of Si$_{136}$ warrants further investigation of this and similar materials for possible thermoelectric applications. In addition, the wide band gap of Si$_{136}$ raises interest for opto-electronics applications.

It is apparent that the properties of type II clathrates are directly dependent on the presence or absence of the guest atoms in the crystallographic voids. It would therefore...
be of interest to study the electrical properties of $M_xE_{136}$ clathrates as a function of the filler content $x$. Ramachandran et al. have synthesized and characterized Na$_x$Si$_{136}$ clathrates for a number of values for $x$ (25), transport properties have not been extensively studied. The synthesis of Ge$_{136}$, the germanium analogue of the unfilled clathrate, would also be a significant result.

ACKNOWLEDGEMENTS

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REFERENCES

Devices and Applications
Dielectric and magnetic materials were developed for use as integrated passive components in LTCC packages. These materials were tested with standard commercially available ESL LTCC tapes as well as those available from Dupont, Motorola and Ferro. ESL conductors were evaluated with all systems and include low cost, high conductivity silver and silver alloys appropriate for high frequency applications. The tapes and pastes were fired using the profiles recommended by the respective tape vendors. All of the ESL compositions are lead free.

The magnetic tapes in the study show permeabilities of 50 to greater than 1200 and were originally developed for use in LTCC transformers and inductors. They are shown here to be capable of decreasing the size of inductors buried in LTCC's. Capacitor tapes and pastes with dielectric constants ranging from 50 - 230 tested as buried capacitors under various processing conditions and temperature coefficients are within the limits of XR7 standards. The compatibility of these inductor and capacitor materials with LTCC tapes from ESL and other vendors is established by evaluating electrical and structural properties.

Introduction:

Indications are that there will be a continuing demand for electronic systems that are less expensive, more reliable, less lossy and capable of providing increased functionality. In addition to these needs, that never seem to be completely satisfied, we believe that many system customers will be asking that their requirements be met with lead-free materials. There is a concern that lead can be leached from discarded electronic equipment and get into the water supply and thus create problems in our ecosystem.

Currently the listed needs, apart from the lead-free materials requirement, are being met by an approach that involves squeezing highly integrated ICs and miniaturized passive components together on a substrate of reduced size. This approach, however, has limitations. One problem is that passive components, which in most cases outnumber the ICs, are reaching a size where difficulties in handling and testing are having an adverse effect on cost and reliability. Another problem is that there is no surface left onto which components can be squeezed.

Designers are turning to approaches that make use of the third dimension, i.e., involve burying components. This paper will discuss an LTCC approach where some or all of the passive components can be buried in the interior of the module leaving room on the surface for ICs which can provide the desired added functionality and increased reliability due to a reduction in the number of solder joints. LTCC technology is especially well suited to the integration of passive components with the package (module) because; (1) its layer by layer build-up scheme provides a number of surfaces on which to deposit components, (2) the LTCC materials are fired at temperatures close to those used to fire thick film passive components, and (3) LTCC host materials not only form an excellent base for the component, they also form a good protective coating.
The LTCC approach also has the necessary flexibility to meet the on-going system needs. Loss can be reduced by proper layout of high conductivity metals and low loss ceramics while the need for low cost is achieved by parallel processing of low cost materials. The concern about lead being leached from discarded electronic equipment is handled through the use of lead free materials.

**Materials and Processing**

The robust set of conductors and dielectric tapes and pastes developed to make the integrated passive parts are listed in Tables 1 and 2. These lead free materials are compatible and cofireable for use in multilayer applications. The conductor system is based on silver which provides high conductivity, low cost, and good solderability. Compatible Au, Pd/Ag and Pt/Ag, pastes are also available where special properties are needed. A wide range of LTCC dielectrics are also available. These include K values up to 16 for size reduction capability[3].

The loss characteristics of these LTCC structural tapes were determined using ring resonator structures. The details of the process and measurement techniques are described in an earlier publication[4]. Silver conductors were used for all test parts. Hold time at peak temperature was varied from 15 minutes to 90 minutes. The heating rate from 450 to 875 was varied from 2°C/minute to 15°C/minute. These parameters were found to have no effect on loss characteristics.

Figures 1 shows loss characteristics for all four LTCC tapes as compared to FR-4. These low and intermediate K dielectric tapes show better loss characteristics than FR-4 and have the additional advantages of higher thermal conductivity and the ability to accommodate multilayer structures.

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Lead Free, Cofireable Conductors</th>
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<tr>
<td>Designation</td>
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<tr>
<td>903-CT-1</td>
<td>High Conductivity Ag</td>
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<tr>
<td>903-CT-1A</td>
<td>Ag Matched for Shrinkage</td>
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<tr>
<td>953-CT-1G</td>
<td>Low Cost Pt/Ag</td>
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<tr>
<td>963-G</td>
<td>Solderable Pd/Ag</td>
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<tr>
<td>902-G</td>
<td>Ag via fill</td>
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<tr>
<td>962-G</td>
<td>Via fill Ag/Au transition</td>
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<tr>
<td>903-CT-A</td>
<td>Solderable top layer Ag</td>
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<tr>
<td>953-AG</td>
<td>Leach Resistant Pt/Ag</td>
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<td>803-MG</td>
<td>Wire Bondable Au</td>
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<td>Solder</td>
<td>95.5 Sn-3.8Ag-0.7 Cu</td>
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<td>9904 Ag*</td>
<td>Top layer photoimageable</td>
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<tr>
<td>8804 Au*</td>
<td>Top layer photoimageable</td>
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<td>41110</td>
<td>K - 4 LTCC Tape</td>
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<td>41020</td>
<td>K - 7.5 LTCC Tape</td>
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<td>41060</td>
<td>K - 16 LTCC Tape</td>
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<td>41250</td>
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<td>41260</td>
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<td>4162</td>
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<td>4163</td>
<td>K - 100 Capacitor Paste</td>
</tr>
<tr>
<td>4164</td>
<td>K - 250 Capacitor Paste</td>
</tr>
</tbody>
</table>

**Buried Capacitors**

Lead free capacitor tapes were developed with a range of K values up to 250. They were tested by embedding them in the four lead-free LTCC host tapes in Table 2 and firing at peak temperatures of 850 - 875 °C. Hold times at peak ranged from 12 to 60 minutes. These same capacitor tapes were also buried in DuPont 951, Motorola T-2000 and Ferro A-6 and except for A-6 fired at a peak temperature of 875°C. The Ferro A-6 was fired at 850°C. All the profiles used were those recommended by the tape vendor. The ESL 41240 (K-50), ESL 41250 (K-100) and ESL 41260 (K-250) tapes were compatible with all the host LTCC tapes. The configuration used for testing these capacitor tapes is shown in Figure 2.
Resulting dielectric constants are shown in Figure 3. Dissipation factor was approximately 1% for most combinations and tended to be lower for the lower K tapes. Temperature variations (TCC) were consistent with X7R characteristics. K values were calculated from measured capacitance values and thickness determined by cross-sectioning the parts. Interface regions were examined for voids and delamination to determine interaction between materials. From this we have determined that the buried capacitor tapes are physically and chemically compatible with a number of commercial LTCC host materials available from different vendors in the marketplace. All the combinations of capacitor and LTCC tapes yielded values for dielectric constant, dissipation factor, and delta C with temperature that were consistent with expected values.

The same electrode was used for all of these test samples, 953-CT-1G (a Pt/Ag conductor with resistivity <6 mohms/square, designed for use with LTCC tapes). It is important to note that the conductor metallurgy can make a difference as seen in Figure 4 where Ag, Pt/Ag and Pd/Ag are compared. These capacitors were buried in ESL 41060-70C (K-16) LTCC tape.

Capacitor tapes have the advantage of uniform thickness which is important for design considerations. Capacitor pastes, however, can be applied in smaller areas as needed. Therefore, capacitor pastes based on the above tape compositions were also buried in these LTCC tapes to establish compatibility. The data obtained on paste buried in LTCC was limited. Table 3 shows some results obtained for capacitor paste buried in ESL 41050-70C (K-13) LTCC tape. A Pt/Ag electrode (953-CT-1G) was used for these experiments.

Figure 5 shows a part prepared by Motorola for evaluation of ESL 4164 (K=250 paste) buried in DuPont 951. Data obtained for this part is shown in Table 4. The silver used was 953-CT-1G and the firing conditions were those recommend fo the 951 tape. The
Table 3

<table>
<thead>
<tr>
<th>Part #</th>
<th>Capacitor Paste Buried in 4.164 LTCC Tape</th>
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<tr>
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<td>Time at 125°C (s)</td>
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<tr>
<td>1462</td>
<td>15</td>
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Table 4

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<td>75.6</td>
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<tr>
<td>60 x 60</td>
<td>156.0</td>
<td>19.5</td>
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</tr>
</tbody>
</table>

Figure 5

4164 Paste Buried in Dupont 951

part (6" x 6") is flat and shows no adverse reaction between the materials from different manufacturers. Warping due to shrinkage mismatch was eliminated by symmetrical design. In a test where only one side was completely covered with capacitor paste with none on the other side, warpage was observed. The amount of warping will depend on the specific design and can be minimized or eliminated with symmetrical placement of constrained shrinkage technology. The high values realized for the dielectric constant provide a route to obtaining small area buried capacitors.

The availability of both high K lead free tape and paste provides the designer with options to take advantage of the uniformity of tape thickness and/or the ability to print paste only where it is needed. Further development of these materials is proceeding for specific customer applications for buried components and will be reported in future papers.

Buried Inductors

Inductors represent another component that designers would like to see removed from the premium surface positions and buried in the interior of the part. This can be done by printing an inductor configuration with thick film conductive coils on standard LTCC dielectric layers. Our objective was to enhance the inductance of such structures by using low temperature cofiring ferrite tapes as the covering dielectric layers. This could result in considerable savings in space and cost.

Permeability of the new tapes was calculated from inductance measurements made on fired toroids formed from laminates of each tape. Grain size measurements was obtained from fracture surfaces on these parts. The permeability vs. firing temperature for the ESL
40010 ($\mu=200$) ferrite tape developed for use in LTCC applications is shown in Figure 6. Similar variation with firing temperature is observed with the ESL 40012 ($\mu=500$) tape. Values of permeability $>700$ are achieved at temperatures compatible with silver conductors (930°C). Permeability of 1100 was obtained with parts fired at 1030°C. All these lead-free tapes exhibit the expected grain size vs. permeability behavior shown in Figure 7 for the ESL 40010 ($\mu=200$) tape. Figure 6 is a photomicrograph of ferrite grains that have been fired at a temperature which yields a permeability value of 1215.

Compatibility testing of the magnetic tape involved sandwiching a conductive silver spiral in ferrite tape layers which were in turn placed in LTCC tape products from ESL, DuPont and Ferro. A typical schematic of this part is shown in Figure 9. Figure 10 presents data showing the increase in inductance resulting from the presence of ferrite tape buried in the LTCC bodies. Examination of the microstructure of these composite structures indicate good compatibility between the LTCC tapes and the ESL ferrite tape. Voids delamination and reaction layers were not observed.

Increasing thickness or the number of ferrite layers increases the inductance. These tapes have been used to manufacture surface mount transformers and inductors\cite{111}. Increasing inductance due to ferrite presence will yield smaller, lighter parts than typical wire wound components. Figure 11 shows comparable transformers made by wire wound and LTCC processing showing that size reduction and shape uniformity are possible with LTCC tape materials and processing.

In order to evaluate the effect of ferrite thickness on inductance, parts were fabricated with spirals buried in tapes with nominal permeability values of 200 (ESL 40010) and 500 (ESL 40012). Inductance should increase with thickness of the ferrite tape up to a point where...
the ferrite could be considered infinite in thickness. At this point, the inductance would be the inductance of the spiral in air times the permeability of the ferrite. This theoretical value for “infinite” thickness is of the order of 2.5 - 5.0 mm for a spiral on top of a slab of magnetic material. Figure 12 shows inductance values increasing in value linearly with thickness for our buried spirals. The $\mu=500$ (ESL 40012) tape yields higher values than the $\mu=200$ (ESL 40010) tape as expected. The effective permeability can be increased by raising the peak firing temperature as shown in Figure 6. The calculated value for inductance of the spiral in air is 1.8 $\mu$H.

Further work is directed at combining magnetic and high K dielectric materials to form modules such as filters. An example of a composite microstructure is shown in Figure 13. The compatibility of the magnetic tape with other dielectric systems is reinforced by the data presented in Figure 9 which shows consistent values for inductance for all tape systems tested.

Summary:
Materials systems were developed for:
- LTCC tapes with loss characteristics better than those achievable with FR-4/Cu technology. The tapes have K values from 4 to 16 which can provide increased signal velocity, better isolation or size reduction with proper material selection.
- Capacitor tapes and pastes suitable for embedding in a variety of LTCC tapes from different
tape manufacturers (ESL, DuPont, Ferro and Motorola).

- A complete lead free materials system including LTCC tape, compatible conductor, embeddable capacitor tapes and pastes, ferrite tapes and solder.
- A wide range of cofireable, low cost, low loss silver based conductors.
- Materials amenable to low cost parallel processing.
- Embeddable capacitor tapes with a K value range of 13-250.
- Inductance enhancing LTCC compatible ferrite tapes with permeabilities attainable from 50 to >1100.

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MEMS IN LOW TEMPERATURE CO-FIRED CERAMICS

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ABSTRACT

The current focus for micro-electromechanical (MEMSs) fabrication is based on the use of Si as the primary material. Great progress has been made due to the extensive processing knowledge in the semiconductor device industry. However, Si based devices have some limitations. Few materials can be integrated into standard IC processing techniques. Multilayer ceramic packaging technology such as low temperature co-fired ceramic materials hold considerable promise as a platform for MEMs devices. In the Ceramic MEMs lab at Boise State University, we are using the LTCC system to build various devices including a simple pressure sensor and an ion mobility spectrometer (IMS). Designs have also been generated for a micro-combustor, micro-propulsion and micro-analytical tools.

MULTI-LAYER CERAMIC SYSTEMS

Ceramic tape technology was developed for efficiently manufacturing interconnects and hybrid microelectronics circuitry through sequential printing and firing of conductor, resistor and/or dielectric paste formulations onto a substrate. The materials system is commonly used for the packaging of microelectronics, particularly in the communications industry. Ceramic tapes can also be used as an efficient and convenient medium for the manufacturing of meso-scale electro mechanical systems because of their many advantages, which include:

- Ease of 3-D multi-layering
- Integration of a wide variety of materials allowing different functions to be incorporated into individual layers, which are then fired into a single substrate.
- Incorporation of device and material characteristics of dielectrics, capacitors, resistors, conductors, magnetic and piezoelectric properties, heating elements, thermal pipes and temperature sensor related functions.
- Easily machined in the green (unfired) state. Size features from 10 microns to 10 mm can be created by mechanical, thermal or chemical means.
- Straightforward integration of other devices including integrated circuits and micro electro mechanical (MEMS) devices out of Si
- Coefficient of thermal expansion closely matches that of Si
• Adaptable to embedded fluidic structures.
• Compatible with harsh thermal and chemical environments
• Robust thermal budget for joining technologies.
• Communication (both fluidic and electronic) between layers by vias
• Rapid prototyping and batch processing for mass production readily available
• Large number of layers can be laminated together (up to 100)
• Fabrication techniques are relatively simple and inexpensive.

Disadvantages of the ceramic systems include:
• Shrinkage during lamination and sintering
• Internal cavities may undergo deformation during lamination and sintering
• High surface roughness
• Features smaller than 10 microns are not currently obtainable.

The most prevalent materials are low temperature co-fired ceramics (LTCC). In the green, pre-fired state, the ceramic tapes consist of alumina particles, glass frit, and organic binder; and they are soft, pliable and easily machineable. Features are machined into the layers and then the circuits are screen printed with metallic, resistor, or capacitor pastes. The layers are then laminated and sintered. During the sintering process, the organic binder volatizes, the glass flows, and the materials harden. For LTCC, the pastes and the tapes are co-fired at approximately 850 °C.

Minimum dimensions of vias and cavities are typically around 100 microns, and are created by using computer numerical control (CNC) punches. Metals, dielectrics, resistors, and magnetic material pastes are deposited in vias by stencil printing, and are deposited on surfaces by screen-printing, or photo-defined imaging processes for smaller features. The vias provide for communication between layers both electronically, when filled with metal, and for fluids if left open. Several materials supplier provide a wide variety of green sheet dielectrics, with co-fireable external and internal conductors and dielectrics, resistors, low melting glasses and brazing materials. The stencil filling and screen-printing processes predominate because they are low-cost. These processes are capable of creating feature sizes of 75 microns or greater. For smaller features, photo-imageable materials are available.

Ceramic multi-layer materials can incorporate micro heat exchanges and heat pipes for thermal control as well as 3-D electronic and fluid paths. Sensors and actuators can be manufactured directly into the tapes.

Materials development within the technology continues as potential new applications are brought to the forefront. Taylor et al. have recently announced the development of photo-imageable green tape.[1] The new tape composition is capable of forming features as small as 50 microns. The photo-imageable tape lends itself to rapid design changes and simultaneously making large and small features. Lautzenhiser and Amaya have demonstrated a material that minimizes lateral tape shrinkage during firing.[2] The tape
only shrinks vertically. Eliminating lateral shrinkage allows the incorporation of additional materials that can be co-fired with the tape.

MEMS APPLICATIONS IN LTCC

Microsystems technology is the miniaturization and integration of electronic functions with microfluidic, photonic, thermonic, and mechatronic functions. The LTCC system has considerable potential as a construction material for meso-scale electro mechanical micro-systems for example chemical and biological reactors, micro-fluidics, miniaturized analysis systems, and miniaturized propulsion systems. Examples of microsystems technologies fabricated in LTCC include a high performance hand-held gas chromatograph developed at Lawrence Livermore National Laboratory[3], as well as lab-on-chip applications such as a MEMS DNA replicator with sample manipulator, and a miniature silicon electronic biological assay chip. Researchers at Sandia National Labs are miniaturizing an Ion Mobility Spectrometer [4] with the target application being detection of explosives for airport security in a device the size of a PDA (personal digital assistant).

The fabrication of liquid flow conduits in ceramic tapes and the measurement of flow in these channels has been demonstrated.[5] Several groups have fabricated magneto-hydrodynamic (MHD) pumps in LTCC. MHD pumps have no-moving parts and can pump in both directions. Bau et al. has demonstrated a mixer or stirrer based on MHD.[6] Sadler et al. has demonstrated an 18 layer device with fluidic channels, integrated electrodes, with inlet and outlet ports for priming the pump with fluids.[7] Channel dimensions were 500 by 500 microns and the overall length of the pump was 24 mm.

Motorola has several projects exploring the use of LTCC for microsystems in wireless, energy and life science applications. A miniature methanol steam reformer has been demonstrated. A miniaturized cyclic continuous flow polymerase chain reaction (PCR) device was developed in LTCC, taking advantage of the vertical micro channel integration capability.[3] PCR is a powerful technique for amplification of a DNA segment for use in DNA fingerprinting and genotyping for disease diagnosis. Vojak and Eden have demonstrated a micro-discharge device in LTCC.[8] Micro-scale gas discharges are potential light sources in the deep UV.

LTCC FABRICATION PROCESS for MEMS

Some modifications to the typical fabrication process may be required depending on the specific device. At Boise State, the fabrication process starts by cutting pieces of tape to a size slightly larger than the desired final size of the device, compensating for shrinkage during firing and trimming. A portion of 951 Green Tape™ is unrolled onto a clean cutting sheet and cut into blanks using an Exacto knife. Cavities, vias, and/or registration holes are then routed in each layer using a BUNGARD CNC-milling machine. Vias are filled with conductive paste using a stencil pattern and knife-blade. An MPS-TF100 thick film screen
printer is then used to print the conductor and resistor pastes required for each layer. The patterned layers are stacked in an alignment tool, collated, and pressed in a PHI SPWR220 hydraulic press with heated plates at 70°C and an applied pressure of 20 MPa (3000psi) for 10 minutes. During lamination, the thermo-plastic organic binder flows and bonds the individual layers, forming a monolithic single unit. If required, the individual devices are then singulated in the green state. The last step of the fabrication process is co-firing the laminated stack, which takes place in a laboratory furnace with a Eurotherm controller. The organic binder is burned away at 350°C, and the LTCC material system is designed to liquid-phase sinter at 850°C.

During sintering, tapes shrink approximately 12 to 15% in the x-y plane and 15% in the z direction. Care during processing can result in shrinkage tolerances of better than ±0.5%. Dimensional changes are taken into account during the design of the part. During the sintering process, the organics are volatized, and the inorganic and metal powders co-sinter to form a dense material structure with the properties of interest. High Temperature Co-fired Ceramics are available which require sintering temperatures of more than 1500°C allowing for an even higher thermal budget.

One of the fabrication challenges is minimizing deformation by sagging for internal cavities. Bau et al.[9] have studied the effect of lamination pressure on deformation as well as the relationship between cavity size and sag during sintering. By reducing the lamination pressure in half, they were able to significantly reduce sag during lamination. Bau controlled the lamination and firing induced deformation through the use of sacrificial materials. The cavities were filled with a combination of organic binder and graphite, which completely burned out during the firing process in an air atmosphere furnace. Espinoza-Vallejos et al.[10] have used carbon black as a fugitive material inside internal cavities.

Another method for preventing collapse of internal cavities, developed by Motorola, is the use of a very thin polymer interlayer that accelerates the bonding between layers, thereby reducing the required lamination pressure. Wilcox et al.[3] demonstrated the use of Poly-2-ethyloxazoline (PEOX) which is a commercially available water-soluble amorphous polymer. Application to the surface of the green sheet reduced the lamination pressure by a factor of five. The glass transition temperature of PEOX is 69 °C. At 5 – 10 °C above the glass transition, the modulus of the polymer drops by several orders of magnitude. The polymer can then flow and enhance the interlayer adhesion. PEOX volatizes during sintering without impacting the fusion of the layers as long as the thickness of the PEOX is kept below 3.0 μm.

LTCC MEMS AT BSU

To demonstrate the capabilities of LTCC for MEMS devices, a capacitive pressure sensor was designed and fabricated.[11] In this device, the change in capacitance between two conductive, parallel plates can be correlated to an applied pressure. In developing this device, the design methodology using SolidWorks and the required data conversion steps...
were established. The ability to use a milling machine to cut LTCC sheets was also developed. The overall process was verified by constructing a successful, working prototype.

To further advance the design and fabrication process, an Ion Mobility Spectrometer (IMS) prototype has been constructed.[12] This device uses multiple concentric rings to generate a constant electric field through a tube. Ions are presented into the electric field at one end and detected at the opposite end. The time required to traverse the length of the tube can be correlated to molecule size, and also chemical species. The LTCC IMS described here was designed for permanent deployment below ground to continuously analyze groundwater. Reduction in size and power consumption of the instrument was made possible by the novel use of LTCC. In developing this device, the design methodology was validated on a more complex system. In fabrication of the device, a new two-step milling process was introduced. The device was constructed from segments cut from previously laminated stacks of sheets. These segments were low pressure bonded using Poly-2-ethylazoxoline (PEOX) to prevent collapse during lamination.

The LTCC IMS device is divided into four sections including the Aperture/Collector, Drift Tube, Tyndall Gate and Ionization Tube. Figure 1 shows a cross-section view of the assembled device.

![Figure 1: The IMS Cross-Section View describes the top-level assembly and approximate size information.](image)

The sections of the IMS are composed of smaller segments which are fabricated using stacks of multiple layers of Du Pont 951 Green Tape. The individual layers in the stacks are screen printed with silver conductor and resistor pastes as required. The layers are then aligned and laminated. Due to manufacturing constraints, the individual segments are limited to a height of 1 cm. The IMS top-level assembly is completed by aligning and stacking...
multiple segments axially and bonding with the PEOX solution. Finally, the assembled device is fired to the final configuration.

Each of the four sections of the IMS was designed individually as 3-D SolidWorks PARTS. To facilitate the manufacturing process and minimize design complexity, common routing and printing patterns were used where possible. The individual segments were then mated in the top level assembly model. Two alignment holes were placed in each segment to orient the parts during assembly. These holes were sized to be used for cartridge heater insertion during operation and testing. All the electrical and CO2 inputs were located in the Aperture/Collector end piece to provide convenient access to housing interfaces. Each of the electrical I/O connections transmits axially through the IMS using internal via circuits. These via paths were coordinated in the model to transmit through each segment to the circuit destination layer. The sample inlet/CO2 exit tube was located in the Ionization Tube segment at the opposite end of the device.

The electrical wiring system of the LTCC IMS begins in the Aperture/Collector segment and traverses the entire device. Several different circuits compose this system. The Drift Voltage circuit begins with an input connection at the Aperture/Collector that travels through the device to the Ionization Tube. The drift voltage is then stepped down by resistors on each layer through the Drift Tube to the Aperture Grid. A conductive ring on each layer is charged by this Drift Voltage circuit to create a constant electric field in the tube. The circuit ends with an output connection at the Aperture/Collector. The Gate function is controlled by a circuit starting with an input connection at the Aperture/Collector and ending by charging a wire grid in the Tyndall Gate section. The Gate voltage is determined by measuring the voltage on a Sense line connected to a junction in the drift voltage circuit immediately preceding the Tyndall Gate section.
The Aperture/Collector segment collects the ionized particles traveling through the Drift Tube and transmits an electrical current signal that corresponds to the arrival of ions. The design of this segment contains a CO2 inlet tube interface for the drift gas, an ion collector plate, an aperture grid and all I/O electrical interfaces between the IMS and the housing.

The Collector plate is formed using a circular disk of conductor printed on the last exposed LTCC layer. The Aperture Grid is fabricated from a .007" thick stainless steel sheet that has been chemically etched to a key-hole shape with small wires suspended across the center section as shown in Figure 3. The attached tab is used for electrical connection. The aperture capacitively decouples the current detected at the collector plate from the approaching ions. This grid is located in a keyhole shaped cutout one layer above the collector plate. After each individual layer is patterned and printed, the layers are stacked with the grid sandwiched into the keyhole cutout. A layer of conductive paste is used on the connection tab to ensure electrical conductivity. This stack is then laminated and assembled into the final device.

The Drift Tube segment generates an electric field that moves the ions from the Ionization Tube to the Aperture/Collector. A series of Green Tape layers is routed with vias alternating from side to side on each successive sheet. A circuit path is printed on each layer including a large circular conduction ring, via connections and embedded resistors as shown in the Figure 4. The sheets are then correlated, stacked and laminated. The sheets then undergo a second routing process to mill the internal core hole to the final diameter. This final cut ensures the voltage rings are exposed to the interior of the Drift Tube for maximum performance. Fourteen segments are then aligned with the Aperture/Collector segment using the two alignment holes and dowel rods. This ensures that the Drift tube core and internal vias are correctly positioned in the assembly. A second group of two segments is used above the Tyndall Gate as part of the Ionization Tube section.
The Tyndall Gate segment generates a perturbed electric field to interrupt the flow of ions through the drift tube. The Gate voltage input circuit is routed in from the Collector end of the IMS. This circuit directly charges the first wire grid (seen in Figure 3) from an external analog circuit. The voltage in the drift tube is tapped off at the junction immediately prior to the first wire grid and routed out the collector end through vias as the Sense Voltage Circuit. This Sense Voltage is used in the analog circuit to determine the required gate voltage input. The drift voltage circuit leaves the junction and flows through vias to the layer housing the second wire grid. This grid is charged with the next successive drift tube voltage progression down to ground. The drift voltage circuit then exits the Tyndall Gate and reenters the Drift Tube progression. The Tyndall Gate assembly showing the two grids and their keyhole shaped housing layers is shown in Figure 5.
The Sense Voltage junction can be seen in the top layer. The Tyndall Gate segment is assembled by stacking the layers shown above and sandwiching the two wire grids as shown. As in the Aperture, a thin film of conductor will be applied to each tab to ensure adequate conductivity in the circuit. The layer stack will then be laminated and bonded in the assembly above the Drift Tube section using the alignment holes shown above and the PEOX solution.

The Ionization Tube segment is used to house the $^{63}$Ni foil in the ionization region and provide flow paths for the sample inlet and CO$_2$ outlet. (Figure 6) The Drift Voltage path illustrated in the Drift Tube segment is continued through the device up to the $^{63}$Ni foil housing. This housing consists of a 1 cm diameter enlarged tube designed to contain the radioactive source material. The Input Drift Voltage circuit is routed through vias to the initial concentric ring. At this point the input via path is connected to the ring and charges the entire downstream Drift Tube array. The Ionization tube region is composed of the three segments shown in Figure 6 all milled from the same substrate and axially bonded into the IMS assembly using PEOX.

As noted, all segments of the IMS are aligned axially using two alignment holes with dowel rods and bonded using PEOX. The assembly is then placed in a laboratory furnace and fired. A furnace stand has been designed to stabilize the stack during this vertical firing position. The DuPont firing profile ramp rates have been lengthened to provide more isothermal heating. The 350°C plateau has been lengthened to allow sufficient organic burn-off prior to sintering at 850°C.

The miniature LTCC IMS device successfully addresses the design requirements for an underground sensor. As noted previously, generating a linear electrical field in previous
IMS devices was difficult due to the perturbations caused by the spaces between voltage rings. Designing a miniaturized IMS device required a fundamentally different approach to take advantage of the strengths of the LTCC material system and provide sufficient accuracy and sensitivity. The layered LTCC approach to constructing devices allows voltage rings to be placed ~0.2mm apart and still maintain large voltage drops through the device. The embedded conductors and resistors are sealed in a hermetic ceramic package that is resistant to the chemicals, moisture and bio-fouling present in the down-hole environment. The embedded elements in the package are more reliable for long term permanent installation. These advantages in addition to the unique LTCC manufacturing process create a capable sensor device for real-world use.

CONCLUSIONS

The devices fabricated by the C-MEMS laboratory demonstrate the abilities of LTCC for fabricating MEMS devices. A complex system can be designed and fabricated successfully. Internal cavities and multi-level channels can be fabricated using the low pressure bonding method. A two-step routing process allows more fabrication flexibility with complex design concepts. The CNC milling process offers versatility for the micro-propulsion device by easily providing multiple prototype nozzle geometries, and providing a smooth, continuous nozzle contour. Some of the potential applications for ceramic MEMS technology include energy scavenging for powering remote devices, miniaturization of chemical analytical techniques, microfluidic designs for packaging of biological sensors, and packaging of sensors and other MEMS components.

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MINIATURIZED SINGLE/MULTI-LEVEL BANDPASS FILTERS
FOR LTCC APPLICATIONS

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Abstract

A simple design methodology for compact folded line bandpass filters in single and multi-level environment is presented. A new stub-loaded folded line configuration with spurious second harmonic suppression is proposed. The design procedure involves representing the folded-line filter section in terms of equivalent admittance inverter network. The design methodology is general and can be extended to other geometries. A six-layer vialess bandpass filter in LTCC is designed to demonstrate the application of the design procedure. Simulation results are validated with full-wave electromagnetic simulation and measurement and the response comparison shows good harmonic suppression.

Introduction

With the increasing demand for high-speed mixed integrated circuits for wireless and mobile applications, higher component densities and compact footprint realization have been gaining prominence in recent years. The emergence of the new system-on-package (SOP) technologies such as multi-layer low-temperature co-fired ceramic (LTCC) [1] and multi-chip module deposition (MCM-D) [2], demand compact high-performance embedded passives for a successful design. In particular, embedded passives in multi-layered media have gained significant importance due to their salient advantages including enhanced performance and lower fabrication costs. Among passive components, bandpass filters are extensively used at RF and microwave frequencies for a host of applications including wireless communication, and test and measurement systems. The challenges involved in the realization of these filters include compact footprint, wide stop band for spurious signal suppression with low pass band insertion loss. The need for "first-time-right" realization of new topologies of bandpass filters suitable for LTCC technology with improved characteristics and compact footprint motivated the proposed research.

Folding a transmission line in single and multilevel environment can effectively reduce the component footprint and has been successfully applied to realize compact RF
coupled-line filters ([3], [4]). For many communication applications, out of band spurious harmonic behavior is becoming a greater concern. Recently, Quendo et al. [5] have suggested integration of low-pass filters in a bandpass filter design. In this paper, design of compact, high performance folded-line bandpass filters with spurious second harmonic suppression is presented. The filters can be realized in a multi-level, multi-conductor transmission line environment suitable for LTCC application. The new filter geometries comprise of bandpass filter sections embedded with lowpass/bandstop filter stub sections in a single/multilevel configuration. For a bandpass filter designed at a center frequency $f_0$, the lowpass/bandstop filter sections consisting of single/coupled open stubs are embedded in the geometry to suppress the second harmonic at $2f_0$ for improved stop band characteristics. A complete synthesis procedure for the filter in terms of equivalent admittance inverter parameters is presented to extract the physical parameters from the given set of filter specifications. To demonstrate the technique, folded-line multiple-coupled bandpass filters are designed with and without second harmonic suppression. The paper will also present the measurement results for the fabricated filters with a comparison with the theoretical results as well as with the full-wave electromagnetic simulation. The results will demonstrate improved stop band characteristics for the new embedded designs.

![Diagram of a multi-level, multi-conductor transmission line system](image_url)

(a) A multi-level, multi-conductor transmission line

![Network representation for a folded-line section](image_url)

(b) Network representation for a folded-line section

Fig. 1 Folded transmission line filter section in a multi-level, multi-conductor environment
**Theory**

Fig. 1a shows a general multi-level multi-conductor transmission line. An N-coupled line system, which represents a 2N×2N port network can be expressed as,

$$[\gamma]_{2N \times 2N} = \frac{1}{\sqrt{\varepsilon_r \varepsilon_0 \mu_0}} \left[ \begin{array}{cc} C\text{coth}(\gamma l) & -C\cos\text{ech}(\gamma l) \\ -C\cos\text{ech}(\gamma l) & C\text{coth}(\gamma l) \end{array} \right]$$

where $C_{N\times N}$ is the capacitance matrix of the N-coupled line structure, $l$ is the length and $\gamma$ is the propagation constant. A folded line can be formed by selectively interconnecting the N-coupled transmission line via small lengths of single or coupled interconnecting transmission lines and corners called sub-networks (Fig. 1b), such that the resulting structure exhibits distinct properties required for a bandpass filter section. The procedure for extraction of reduced port network parameters is similar to the approach described in [6] for the single and coupled folded-line structures. The circuit parameters of an N-coupled transmission line system described in terms of the 2N-port network can be determined using the modeling approaches reported in the literature [7-9]. The N-coupled transmission line network can be reduced to a 2-port network exhibiting bandpass filter property by selectively interconnecting the leads while leaving some open-circuited. The choice of interconnection and open-circuit termination can result in diversified filter properties for the reduced 2-port network. This procedure enables the designer to take into account the effect of the interconnecting lengths of the transmission line section during the course of the design.

![Fig. 2 Equivalent circuit representation](image)

**Filter Design Procedure**

The bandpass filter design procedure is based on equivalent circuit approach shown in Fig. 2. In this approach, a multiple-coupled line filter section illustrated in Fig. 1(b) is visualized as an equivalent parallel-coupled line filter section giving nearly the same...
filter properties. The aim is to realize the physical parameters, such as the strip width and the separation between conductors of the multiple-coupled section, by matching the equivalent admittance inverter network parameters with those calculated for the conventional parallel-coupled section. In Fig. 2b, the π-network consisting of the three susceptances, \( B_a, B_b \) and \( B_c \) can be extracted from the two-port admittance parameters of the folded-line filter section. The equivalent admittance \( (J) \) inverter network shown is represented in terms of a π-network sandwiched between two transmission lines of electrical length \( \phi_1 \) and \( \phi_2 \) as shown in Fig.2. By comparing the two equivalent circuits given in Figs 2a and 2b, the admittance inverter parameter \( J \), and the equivalent electrical lengths \( \phi_1 \) and \( \phi_2 \) can be determined from the equations given in [10], [11].

Fig. 3 Single and multi-level Bandpass folded line filter sections

(c) Multilevel- folded line filter sections

Fig. 3 shows some possible configurations for folded line bandpass filter sections realized in single and multi-level environment. In Fig. 3a, the folded line filter section is formed by using a coupled 4-line with interconnecting curved sections and open circuit terminations. The structure shown in Fig. 3b is similar to that shown in Fig. 3a, except that it has an additional shunt stub to suppress the second harmonic suppression. This stub acts as embedded bandstop section and by suitable choice of the length and width of the individual stubs for each filter section, the second harmonic frequency can be effectively suppressed. Fig. 3c shows some multi-level filter sections that can be realized using the design procedure.
The filter design procedure for the folded line filters can be explained as follows: For the given filter specifications such as number of resonators, type of the filter such as maximally flat or Chebyshev, bandwidth and center frequency, the lowpass filter prototype values are first determined. Next, the required J-inverter values for each filter section are computed using the equations given in [10]. The physical parameters such as conductor width and spacing between conductors are optimized to get the desired value of J for each section maintaining the sum of the two equivalent phase delays, $\phi_1 + \phi_2 = \pi$.

In order to design the bandpass filter with embedded bandstop stub element, first the folded line filter without the stub loading is designed. Individual stubs are inserted between the filter sections with initial lengths being a quarter-wave length at twice the center frequency of the bandpass filter. The lengths and widths of the stubs are then optimized to achieve the desired stop band response with harmonic suppression. Since the insertion of the stubs can marginally affect the pass band response of the filter, a second level tuning is carried out for the individual filter sections with the stub included as a part of each filter section to achieve the necessary values of J-inverter parameters and phase delays corresponding to the filter initial design. This can be carried out without changing the stub parameters. The tuned filter sections, when cascaded will give the final filter response with the desired harmonic suppression.

![Graph showing filter response](image)

**Fig. 4 Response for the bandpass filters designed (layout in Fig. 5) using the filter sections shown in Fig. 3a and Fig. 3b**
Results

To demonstrate the feasibility of the proposed configurations, both configurations of folded-line bandpass filters using the filter sections shown in Figs. 3a and 3b were designed at 1.5 GHz using the procedure explained in the previous section. A four-section maximally flat design with a fractional bandwidth of 0.1 was considered. The design was carried out on a microstrip configuration with $\varepsilon_r=2.2$ and dielectric thickness, $h=62$ mil. From the filter theory, the J-inverter parameters for each section have been computed. For the same passband characteristics, the four-section filter was realized in both configurations shown in Figs. 3a and 3b. Curved line sections have been used as the interconnecting lengths to minimize the discontinuity effects. The simulated response for both the filters is shown in Fig. 4. It can be seen from the plot that for the folded-line structure without any stubs shown in Fig. 3a, the first higher order harmonic appears around a frequency of 2.9 GHz. For the modified filter shown in Fig. 3b, this harmonic has been suppressed. The simulated response for the second configuration is compared with the full-wave Momentum simulation and the response is plotted in Fig. 4. The simulated results show good agreement. The layouts for the filters generated by the full-wave electromagnetic simulator [12] are shown in Fig. 5.

![Fig. 5 Layouts for the designed folded line bandpass filters](image)

To further validate the theory by measurement, the new folded line filter geometry with harmonic suppression was fabricated with the final layout shown in Fig. 3b. The filter was designed using RT-5880 Duroid dielectric substrate with a thickness of 62mil and was tested on an HP8722 vector network analyzer. The measured insertion loss and return loss are shown in Fig. 4 for a comparison with the theoretical results. The measured response is found to be in good agreement with the proposed theory and demonstrates the second harmonic suppression. A photograph of the fabricated filter is shown in Fig. 6.
To demonstrate the application of folded line filters to the LTCC technology, a six-level via-less bandpass filter was designed at 2 GHz. Simulations were carried out using a dielectric material from Dupont (951 AT tape) with a dielectric constant of 7.8. The six dielectric layers have been chosen with thicknesses of 7.2, 3.6, 10.8, 10.8, 3.6 and 7.2 mils respectively. The bandpass filter was designed using the design procedure explained in the previous sections at a center frequency of 2 GHz. A schematic layout of the vialess filter is shown in Fig. 7. The response of the filter is shown in Fig. 8.
Conclusion

A new simple design methodology for a variety of compact folded-line coupled bandpass filters realized in a multi-layered environment has been presented. An equivalent admittance parameter network approach has been proposed to synthesize a variety of compact filter structures. An embedded shunt stub design to suppress second harmonic in the bandpass filter response has been proposed. To demonstrate the design feasibility, a 4-section maximally flat filter design has been carried out with and without the embedded stub and a comparison of the responses has been presented. The results are validated with the help of full-wave electromagnetic simulation and experiment. The results show very good agreement. To demonstrate the application to LTCC, a six-layer vialess bandpass filter is designed at 2 GHz and the response and layout for the filter have been presented. The new filter configurations offer distinct advantages such as low insertion loss, compact footprint, design feasibility in terms of realizable physical dimensions and implementation for a host of embedded passive and LTCC applications in the frequency range of 1 to 10 GHz.

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